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ARCHITECTURAL ALTERNATIVES TO IMPLEMENT HIGH-PERFORMANCE $\Delta\Sigma$ MODULATORS

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Cette thèse intitulée :

ARCHITECTURAL ALTERNATIVES TO IMPLEMENT HIGH-PERFORMANCE $\Delta\Sigma$ MODULATORS

présentée par : HONARPARVAR Mohammad
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DEDICATION

To my Mother and Father,
To Elham.

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RÉSUMÉ

Le besoin d'appareils portatifs, de téléphones intelligents et de systèmes microélectroniques implantables médicaux s'accroît remarquablement. Cependant, l'optimisation de l'alimentation de tous ces appareils électroniques portables est l'un des principaux défis en raison du manque de piles à grande capacité utilisées pour les alimenter. C'est un fait bien établi que le convertisseur analogique-numérique (CAN) est l'un des blocs les plus critiques de ces appareils et qu'il doit convertir efficacement les signaux analogiques au monde numérique pour effectuer un post-traitement tel que l'extraction de caractéristiques. Parmi les différents types de CAN, les modulateurs Delta Sigma ($\Delta\Sigma$M) ont été utilisés dans ces appareils en raison des fonctionnalités alléchantes qu'ils offrent. En raison du suréchantillonnage et pour éloigner le bruit de la bande d'intérêt, un CAN haute résolution peut être obtenu avec les architectures $\Delta\Sigma$. Il offre également un compromis entre la fréquence d'échantillonnage et la résolution, tout en offrant une architecture programmable pour réaliser un CAN flexible. Ces CAN peuvent être implémentés avec des blocs analogiques de faible précision. De plus, ils peuvent être efficacement optimisés au niveau de l'architecture et circuits correspondants. Cette dernière caractéristique a été une motivation pour proposer différentes architectures au fil des ans.

Cette thèse contribue à ce sujet en explorant de nouvelles architectures pour optimiser la structure $\Delta\Sigma$M en termes de résolution, de consommation d'énergie et de surface de silicium. Des soucis particuliers doivent également être pris en compte pour faciliter la mise en œuvre du $\Delta\Sigma$M. D'autre part, les nouveaux procédés CMOS de conception et fabrication apportent des améliorations remarquables en termes de vitesse, de taille et de consommation d'énergie lors de la mise en œuvre de circuits numériques. Une telle mise à l'échelle agressive des procédés, rend la conception de blocs analogiques tel que un amplificateur de transconductance opérationnel (OTA), difficile. Par conséquent, des soins spéciaux sont également pris en compte dans cette thèse pour surmonter les problèmes énumérés.

Ayant mentionné ci-dessus que cette thèse est principalement composée de deux parties principales. La première concerne les nouvelles architectures implémentées en mode de tension et la seconde partie contient une nouvelle architecture réalisée en mode hybride tension et temps. Les CAN proposés sont implémentés en circuits à capacités commutées tout en présentant une solution pour surmonter les limites citées précédemment. Un amplificateur à base d'onduleur est proposé pour réaliser les intégrateurs réquis pour construire un modulateur delta sigma ($\Delta\Sigma$M). On montre que l'OTA proposé est suffisamment robuste par rapport

Processus voltage et température (PVT). Pour la deuxième partie de la thèse, il est démontré que le mode hybride (tension et temps) est une approche bénéfique pour mettre en œuvre un $\Delta\Sigma$M. Par conséquent, un oscillateur en anneau à temps continu basé sur l'architecture MASH $\Delta\Sigma$M est ciblé pour la deuxième partie de la thèse. On montre que le budget de puissance du $\Delta\Sigma$M est principalement limité par les OTA nécessaires à la réalisation du filtre de la rétroaction du circuit. Pour s'attaquer à ce problème, une partie de la conception est transférée dans le domaine temporel afin de tirer parti des avantages de la réduction de l'échelle technologique. De plus, la solution hybride proposée facilite l'implémentation du $\Delta\Sigma$M.

ABSTRACT

The need for hand-held devices, smart-phones and medical implantable microelectronic systems, is remarkably growing up. However, keeping all these electronic devices power optimized is one of the main challenges due to the lack of long life-time batteries utilized to power them up. It is a well-established fact that analog-to-digital converter (ADC) is one of the most critical building blocks of such devices and it needs to efficiently convert analog signals to the digital world to perform post processing such as channelizing, feature extraction, etc. Among various type of ADCs, Delta Sigma Modulators ($\Delta\Sigma$Ms) have been widely used in those devices due to the tempting features they offer. In fact, due to oversampling and noise-shaping technique a high-resolution ADC can be achieved with $\Delta\Sigma$ architectures. It also offers a compromise between sampling frequency and resolution while providing a highly-programmable approach to realize an ADC. Moreover, such ADCs can be implemented with low-precision analog blocks. Last but not the least, they are capable of being effectively power optimized at both architectural and circuit levels. The latter has been a motivation to proposed different architectures over the years.

This thesis contributes to this topic by exploring new architectures to effectively optimize the $\Delta\Sigma$M structure in terms of resolution, power consumption and chip area. Special cares must also be taken into account to ease the implementation of the $\Delta\Sigma$M. On the other hand, advanced node CMOS processes bring remarkable improvements in terms of speed, size and power consumption while implementing digital circuits. Such an aggressive process scaling, however, make the design of analog blocks, e.g. operational transconductance amplifiers (OTAs), cumbersome. Therefore, special cares are also taken into account in this thesis to overcome the mentioned issues.

Having had above mentioned discussion, this thesis is mainly split in two main categories. First category addresses new architectures implemented in a pure voltage domain and the second category contains new architecture realized in a hybrid voltage and time domain. In doing so, the thesis first focuses on a switched-capacitor implementation of a $\Delta\Sigma$M while presenting an architectural solution to overcome the limitations of the previous approaches. This limitations include a power hungry adder in a conventional feed-forward topology as well as power hungry OTAs. An inverter-based amplifier is also proposed to realize the integrators of the switched-capacitor $\Delta\Sigma$M. It is shown that the proposed OTA is robust enough over process, voltage and temperatures (PVTs). For the second part of the thesis, it is demonstrated that a hybrid voltage and time domain is an acceptable venue to implement

a $\Delta\Sigma$M. Therefore, a continuous time gated ring oscillator based MASH $\Delta\Sigma$M is targeted for the second part of the thesis. It is shown that the power budget of $\Delta\Sigma$Ms is mostly limited by the operational amplifiers required to realize the loop filter. To tackle this issue, part of the design is shifted to the time-domain to take the advantages of a scaling friendly environment. Moreover, the proposed hybrid solution eases the implementation of the $\Delta\Sigma$M.

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LIST OF ABBREVIATIONS

AAF	Antialiasing filter
ADC	Analog-to-digital converter
BP	Band-pass
BPF	Band-pass filter
CMFB	Common-mode feedback
CMOS	Complementary MOSFET
CT	Continuous-time
CT-DSM	Continuous-time delta sigma modulator
DAC	Digital-to-analog converter
DCL	Digital cancelation logic
DEM	Dynamic element matching
DNL	Differential nonlinearity
DR	Dynamic range
DSP	Digital signal processor
DT	Discrete-time
CT-DSM	Discrete-time delta sigma modulator
DWA	Data weighted averaging
ENOB	Effective number of bits
FFT	Fast Fourier transform
FOM	Figure of merit
FS	Full scale
GRO	Gated ring oscillator
IBN	In-band noise power
IIT	Impulse-invariant transformation
MASH	Multi-stage noise shaping
MOSFET	MOS field-effect transistor
OTA	Operational transconductance amplifier
PWM	Pulse-width modulation
SAR	Successive approximation register
SC	Switched-capacitor
SMASH	Sturdy multistage noise shaping
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise-plus-distortion ratio

SQNR	Signal-to-quantization-noise ratio
SR	Slew rate
SRO	Switched ring oscillator
STF	Signal transfer function
TDC	Time-to-digital converter
TEQ	Time-encoding quantizer
THD	Total harmonic distortion
VCO	Voltage-controlled oscillator
PVT	Process, Voltage, Temperature

CHAPTER 1 INTRODUCTION

1.1 Motivation

The electronics of a general biomedical device, as illustrated in Figure 1.1, consist of energy delivery, analog to digital converter (ADC), digital signal processor (DSP), and communication subsystems and each of these building blocks must be designed for higher reliability and lower power consumption. Among all mentioned blocks, ADCs play a crucial role since physical biomedical signals are analog and they need to be digitized before they can be processed digitally to take advantage of the sophisticated capabilities of a DSP. ADC requirements depend on system characteristics, namely bandwidth and dynamic range and its performance must be optimized in terms of power consumption since it can be a significant portion of the total power budget. Table 1.1 lists some examples of existing and emerging applications for biomedical devices while emphasizing on the ADC requirements [1]. As can be seen from this table, the ADC must cover the range of a few kHz signal bandwidth (for body-area monitoring) to tens of MHz for biomedical ultrasound beamformers while offering 8-12 bit resolution for various applications. For the rest of this thesis, two ADCs are targeted. One is a 14-bit low bandwidth (LBW) ADC with 20 kHz signal bandwidth and sub-100 μ W power consumption the other is a wide bandwidth (WBW) ADC to cover 10 MHz signal bandwidth. It is worth mentioning that the first one is implemented in the voltage domain while the latter is realized in a hybrid voltage and time domain.

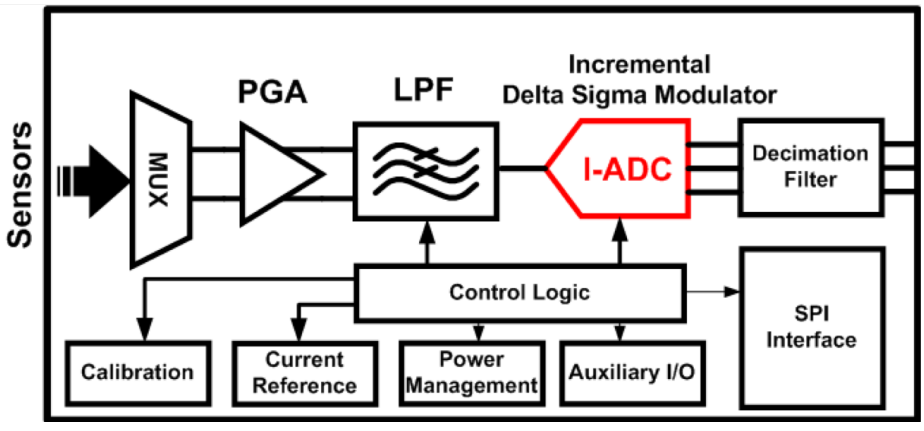


Figure 1.1 Conceptual diagram of a generic biomedical device

Table 1.1 Examples of existing and emerging applications for biomedical devices [1]

Application	power	ADC/DAC	Processor	Comunication	Energy source
Pacemaker	$< 10\ \mu$W	1 kSPS, 8b ADC	1 kHz DSP	Inductive, link	10-year lifetime, battery
Body-area monitoring	140 μW	1 kSPS, 12b ADC, per channel	< 10 MHz DSP	Far-field wireless, link	Battery
Analog cochlear processor	200 μW	16, 1 kSPS, 8b ADCs	Analog DSP	Inductive, link	1-week lifetime, rechargeable battery
Hearing aid	100-2000 μW	16 kSPS, 12b ADC	32,kHz-1MHzDSP	Tele-coil	1-week lifetime, rechargeable battery
Sensory applications	$100< \mu$W	20 kSPS, 12-14b ADC	NA	NA	1-week lifetime, rechargeable battery
Neural recording	1-10 μW	Up to 1000s of channels, 100 kSPS, 8b ADC	NA	High rate, inductive link	Inductive, power
Retinal stimulator	250 mW	10 kSPS, 4b DAC, per electrode	No embedded DSP	High rate, inductive link	Inductive, power
Biomedical ultrasound	$< 10\ m$W	1200 MSPS	NA	NA	1-week lifetime, rechargeable battery

1.2 Problems statement

1.2.1 LBW ADCs limitations

Ongoing researches have been performed on the integration of the microelectromechanical systems (MEMS) devices with the analog front end (AFE) including MEMS transducer and ADCs. Figure 1.2 illustrates the block diagram of an on-chip sensor interface. Since the output of sensor transducer is a very weak signal the AFE must be carefully designed to handle such a signal in micro volt range. One of the most critical part of an on-chip sensor interface, is a high performance sub-microwatt ADC to deliver a high quality data to the DSP for post processing [2].

Delta-sigma modulators ($\Delta\Sigma$Ms) are widely preferred in analogy with the Nyquist rate ADCs because of the following reasons :

1. $\Delta\Sigma$Ms are well-suited to achieve high resolution (14-24 bit) in the band of interest without stringent matching requirement or calibration rather than the Nyquist rate ADCs [3].
2. $\Delta\Sigma$Ms could be implemented with low precision analog blocks. In other words, this kind of ADC is quit robust against circuit imperfections.
3. Intrinsically linear mono-bit quantizer could be utilized to get rid of the matching requirement and as a consequence drastically reducing the power consumption.
4. Most of the signal processing take to the reliable/flexible digital domain by employing $\Delta\Sigma$Ms so that the power consumption could be reduced severely by scaling down the technology and supply voltage.

Regarding above brief, it is essential to design a high resolution (14-bit) low power (less

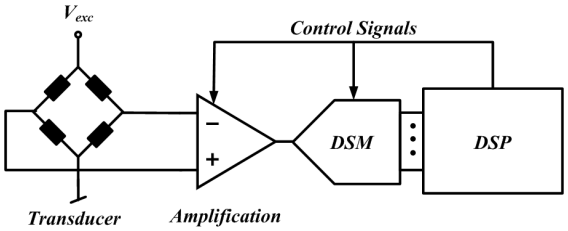


Figure 1.2 Block diagram of a smart sensor chip, [2] (©[2005] IEEE)

than 100-μW) ADC while considering both system and circuit level technics. In terms of system level design, there are two architectures to implement a $\Delta\Sigma$M. 1) Feedback (FB) topology. 2) Feed Forward (FF) topology [4]. FF topology is preferred because of the following reasons. First of all, FF topology presents lower integrators output swing in analogy with FB topology. Second, the number of feedback DAC in the FF topology is less than FB counterpart. However, FF topology suffers from a power consuming adder before the quantizer and out of band peaking in the STF, as well [5]. Therefore it is important to find a solution to get rid of the power hungry adder in the FF architecture. At the circuit level point of view, the OTA, apparently, is the main block in a discrete time (DT)-$\Delta\Sigma$M.

1.2.2 WBW ADCs limitations

As mentioned in the previous section, an ADC with a 10-MHz signal bandwidth (referred as WBW) with a resolution of more than 12-bit, which translates into more than 75-dB SNDR, is considered for the second part of this proposal. It is a well-established fact that $\Delta\Sigma$M is a unique option for targeted resolution and an acceptable figure of merit (FOM), as can be concluded from Figure 1.3. Essentially two scenarios are available to realize a $\Delta\Sigma$M. 1) DT or switched capacitor (SC) implementation. 2) continuous time (CT) implementation. Having a glance at Figure 1.4, CT-$\Delta\Sigma$M is well-suited for high bandwidth applications because of the following justifications. 1) SC-$\Delta\Sigma$Ms need amplifiers with high unity gain bandwidths (usually at least five times of the sampling frequency) to satisfy the settling accuracy requirements while no settling behavior is involved in CT-$\Delta\Sigma$Ms which make them operate at higher sampling rate and/or with less power consumption. 2) Inherent anti-aliasing filtering is another unique feature of a CT-$\Delta\Sigma$M since the input signal is sampled at the output of CT loop filter hence significant suppression at the aliasing frequencies can be achieved. 3) For the SC-$\Delta\Sigma$M, design of the sampling network at the input of the modulator is a challenging task since sampling accuracy greater than the full resolution of the entire modulator is needed [8]. However, in the case of CT-$\Delta\Sigma$M sampler is inside the loop filter and any error caused by

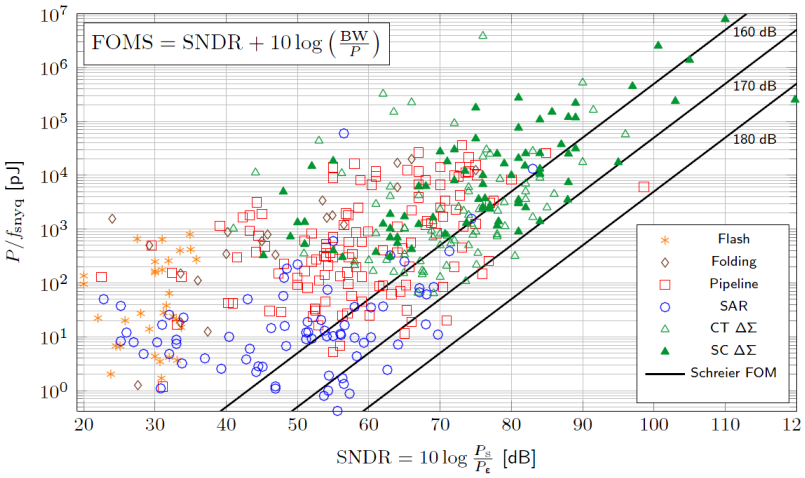


Figure 1.3 Figure of Merit (FOM) against SNDR for various ADC architectures[6, 7] (©[2016] IEEE, ©[2016] IEEE)

sampling process accompany with quantization noise is easily suppressed by the gain of the loop filter in the desired bandwidth. However, CT-ΔΣMs suffer from clock jitter rather than SC-ΔΣMs. Although any timing error, injected to the sampler, is suppressed by the gain of loop filter, timing error of the feedback DAC is directly injected to the modulator input without any noise shaping and this effect significantly degrades the SNR of the modulator. Therefore, this effect must be minimized for high performance ΔΣMs. Another drawback of the CT-ΔΣMs is the excess loop delay (ELD). Performance degradation and even instability may occur if the excess loop delay is too large. Fortunately, this effect can be alleviated by proper employing of ELD compensation techniques [9].

Regarding above explanations, A ΔΣM, implemented in the CT regime, is opted for this research. But there is still some bottlenecks need to be carefully addressed. These bottlenecks are itemized as follows :

1. It is emphasized that CT-ΔΣM would be a good option for the wide bandwidth applications where active-RC, gm-C, and MOSFET-C integrators are usually utilized to implement the loop filter of the modulator [4]. In the voltage/current domain, operational amplifiers (op-amps) or operational transconductance amplifiers (OTAs) consume most of the power budget. Moreover, either lack of enough voltage headroom in the advanced node technologies (65 nm CMOS process and beyond) or shrinking the nominal voltage rate exacerbates the issues. A solution to this problem is to shift part of the design from voltage/current mode signal processing to the time mode signal processing [11]. There are two main benefits behind the time domain approaches. First there is no longer any concern related to the swing problems since the voltage/current

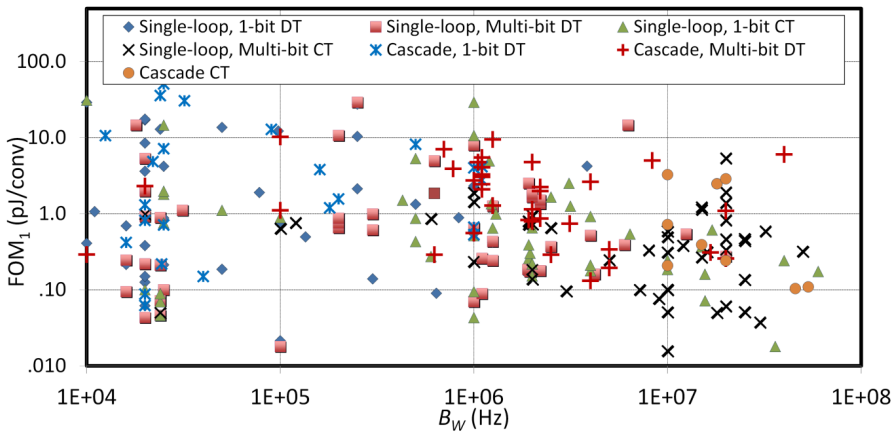


Figure 1.4 FOM$_1$ ($FOM_1 = \frac{P(W)}{2^{ENOB(bit)}.output\ rate(S/s)}$) against BW for various types of ΔΣMs [10](©[2018] John Wiley and Sons)

swing is translated into the time difference. Second, we can take the advantages of the digitally implementation of the analog blocks [12].

2. VCO-based quantizer ($VCOQ$), which is considered as one of the time mode approaches, is an appealing option to implement part of a CT-ΔΣM with it. However, this architecture suffers from severe non-linearity caused by voltage to frequency characteristics of the VCO. Multiple approaches have been addressed to linearize it and enhance the dynamic range [13]. These approaches can be categorized into embedding the VCOQ in a ΔΣM loop or digitally calibrating the VCOQ non-linearity. In the first approach, a high-order ΔΣM with power hungry op-amp is needed while digital calibration makes the system power consuming due to high speed look-up tables (LUTs) high sampling rate.

3. As mentioned earlier, higher order modulator, which is severely susceptible to instability, is needed for embedded VCOQs. To overcome this issue, multi stage noise shaping (MASH) ΔΣM is an alternative. However, quantization noise must be extracted in a voltage/current domain and it adds circuit complexities. It will be shown that the quantization error can be extracted in a time domain with a simple digital circuit.

1.3 Research objectives

1.3.1 LBW ADC research objectives

To tackle the aforementioned problems in Section 1.2.1, an alternative is targeted in which the power hungry adder is eliminated. It is also planned to propose a power optimized fully

differential OTA. Therefore, it is worth investigating the new generation of the OTAs i.e. inverter-based OTA. To diminish the power consumption proper techniques must be adapted. Reducing the supply voltage is one of the solutions to do so. Reducing the supply voltage, however, has its own drawbacks e.g. lower voltage headroom. Therefore, an appropriate technique must be chosen to alleviate those issues. Biasing the OTAs in the weak inversion is an appealing solution to lower the power consumption as well. However, circuits biased in the weak inversion are sensitive to the PVT variations. Self-biasing techniques could fix such an issue. Having had above discussion, the main objectives of this research are itemized as follows :

1. Our goal is to address a new DT-MASH $\Delta\Sigma$M which satisfies the main requirements of a LBW ADC in terms of resolution and power consumption.
2. High-level synthesis must be performed to avoid over-designing and thus to optimize the design parameters.
3. New FF structure is proposed and quantization noise extraction is only performed by the available analog signals at the output of the integrator used in the proposed modulator.
4. In terms of circuit level technics, enough effort must be made on OTA selection since the OTAs are the most momentous part of a DT-$\Delta\Sigma$M.

1.3.2 WBW ADC research objectives

The strategy to tackle the aforementioned limitations in Section 1.2.2 is to propose a CT gated ring oscillator (GRO)-based MASH (*CG-MASH*) structure. MASH structures are sensitive to the mismatch between analog coefficients and digital cancellation logic. Therefore, a high-gain operational amplifier is required to alleviate this effect. Quantization error extraction is another challenge in a CT MASH $\Delta\Sigma$M. Therefore, proper quantization error extraction technique is required. That being said, the main objectives are listed as follows.

1. We plan to introduce a new CG-MASH $\Delta\Sigma$M which is well-suited for high bandwidth applications. This also demonstrates a significant improvement compared to DT-MASH, single loop CT-$\Delta\Sigma$M with the same noise shaping capability and CT-MASH $\Delta\Sigma$M.
2. Locate the main challenges and their solutions of the proposed CG-MASH in high level syntheses. Architectural level solutions are explored to overcome these challenges.
3. Use analog filter to delay and remove the quantization error of the first stage is addressed by using simple digital delay due to time nature of the quantization error in the proposed architecture.

1.4 General organization of the thesis

The main challenges of SC-ΔΣMs as well as VCO-based ΔΣMs are reviewed in Chapter 2. As explained, SC-ΔΣMs with distributed feed forward paths suffer from a power-hungry adder located before the quantizer. Although, a passive adder can be used to save power, it is at the expense of pushing stringent requirements on the second OTA in the second order ΔΣM. A comprehensive literature review is also performed in Chapter 2. The main drawbacks of the VCO-based quantizer is scrutinized and the main techniques to overcome the drawbacks are also reviewed.

This thesis is based on three journal papers to address mentioned drawbacks in Chapter 2. The first journal, which is presented in Chapter 3, mainly explores a new architecture to eliminate the power hungry-adder in a conventional feed forward topology. To do so, an adder-less SC-ΔΣM is proposed and MASH structure ΔΣM is formed based on the adder-less topology. A self-biased inverter-based OTA is then introduced where it is biased in the weak-inversion region. It is demonstrated that the OTA fails over slow process corners and low-supply voltage. To cope with that issue, a self and body biased inverter-based OTA is proposed.

Chapter 4 represents the second journal paper. During the research process, it is found that MASH ΔΣMs are susceptible to the mismatch between analog loop filter and the digital cancellation logic. To overcome such a drawback, a modified SMASH ΔΣM is proposed. The proposed SMASH ΔΣM offers a better linearity compared to the conventional SMASH architecture. It also needs relaxed OTA DC-gain requirements.

Chapter 5 represents the third journal paper. It scrutinizes a new trend in the hybrid ΔΣMs. The high-level synthesis of the proposed continuous time gated ring oscillator based MASH ΔΣM is first presented. Main circuit imperfections are described as well. Chapter 5 then continues with the circuit level implementation of the proposed modulator as well as measurement results.

Chapter 6 provides a general discussion on the proposed ΔΣMs. It describes the main features of the proposed ΔΣMs. Final conclusion, main contributions of this research as well as suggestions for future work are all drawn in Chapter 7.

CHAPTER 2 LITERATURE REVIEW

As mentioned in the previous chapter, analog to digital converter (ADC) is one of the most crucial blocks in many electronic devices. ADCs are essentially categorized into the Nyquist rate ADCs as well as over-sampled and noise-shaping ADCs. Nyquist rate ADCs are not suitable options for high-resolution applications and even they are over-sampled, in many applications, to provide a medium resolution and relax the filtering requirements. Over-sampled and noise-shaping ADCs, known as $\Delta\Sigma$ ADCs, however provide special features over the Nyquist rate ADCs. Such ADCs can provide medium to high resolution with low precision building blocks. They also compromise between resolution and bandwidth. They can also be optimized at both system level and circuit level. This chapter, which focuses on the $\Delta\Sigma$ ADCs, is split into two main sections. In the first section, our literature review is mainly focused on the low bandwidth (less than 20 kHz) DT(SC)-$\Delta\Sigma$Ms which is truly the foundation of the first proposed LBW $\Delta\Sigma$M presented in the next chapter. The second part of this chapter is dedicated to WBW $\Delta\Sigma$Ms. Therefore, hybrid voltage and time modes $\Delta\Sigma$Ms are comprehensively reviewed.

2.1 Literature on LBW SC-$\Delta\Sigma$Ms

Many state of the art high resolution low bandwidth (less than 25 kHz) modulators have been introduced. Single stage $\Delta\Sigma$Ms have been presented in [14–17] and [5] while MASH $\Delta\Sigma$M for low bandwidth applications have been presented in [18, 19]. A fourth order single stage $\Delta\Sigma$M has been introduced in [20] which took the advantage of the low-threshold voltage devices of a 0.13 μm CMOS process to operate at 1 V supply voltage. It is worth noting that single stage higher order (third order and more) modulators are severely susceptible to instability and the maximum out-of-band gain ($Hinf$) of the NTF needs to be selected meticulously. Moreover, the modulator in [20] implemented as a fourth order FF structure and as will be described in the rest of this proposal, the power hungry adder is the main bottleneck of the FF structure which was resolved by employing the passive adder. This technique suffers from reducing the signal swing at the input of comparator and capacitors mismatch as well. Similar strategy has been adopted in [16] in which a 1.5 bit, fourth order FF structure was proposed for 20 kHz signal bandwidth. To resolve the problem of summation block, a switch matrix feedback compensation based on a direct summation technique [15] was adapted. Such a technique is well-suited for multi bit quantizer and not applicable for mono bit quantizer $\Delta\Sigma$Ms. Employing the multi bit quantizer itself has its drawbacks. Dynamic Element

Matching (DEM) technique needs to be utilized to mitigate the non-linearity problem of the DAC in the feedback path which obviously leads to the circuit complexity as well as power consumption.

2.2 Literature on WBW ΔΣMs

2.2.1 ΔΣMs with time-domain blocks

There are three common ways to represent a signal in electronic circuits ; Continuous Time Continuous Amplitude (CTCA), Discrete Time Discrete Amplitude (DTDA) and Discrete Time Continuous Amplitude (DTCA). Using time resolution of digital waveform to represent signals introduces the fourth way of signal representation i.e. Continuous Time Discrete Amplitude (CTDA). There are two main benefits behind using this approach in today's electronics. First, the power dissipation follows the rule of CV^2f, which is the power dissipation of a digital gate driving a load capacitance (C) and switching between 0 to V at the sample rate of (f). The second benefit is that the supply voltage is virtually uncoupled from SNR since the signal swing is no longer represented in the voltage mode and it is in the time domain, instead. This feature is very important either for advanced node technology with low supply voltage ($V_{dd} < 1V$) or for the circuits operating at the fraction of nominal voltage rate. This also makes the circuit dissipate less power in analogy with conventional voltage mode circuits. However, time domain circuits suffer from timing jitter since the representation in the time domain. To have a better insight, a comparison is performed for a unity gain buffer corresponding to the Figure 2.1 [21].

Assuming that the digital waveform has the slop of V_{dd}/t_r for the rising and falling edge, standard deviation of the voltage error is expressed by v_σ and t_σ stands for standard deviation of the timing error, t_σ can be expressed as follow :

$$t_\sigma = \frac{v_\sigma}{dv/dt} = \frac{v_\sigma t_r}{V_{dd}} \tag{2.1}$$

For a CTDA signal with two transitions in every clock period (T_s) the upper limit of SNR in the time domain is given by :

$$SNR_T = \frac{T_s^2}{16t_\sigma^2} \tag{2.2}$$

Also the upper limit SNR for the voltage mode can be expressed as :

$$SNR_V = \frac{V_{dd}^2}{8v_\sigma^2} \tag{2.3}$$

Therefore,

$$\frac{SNR_T}{SNR_v} = \frac{T_s^2}{2t_r^2} \tag{2.4}$$

For the sampling frequency of 640 MHz and rise time of 28 pS, CTDA provides 63 dB SNR better than CTCA. Time to digital converters were originally proposed to measure single-shot pulses in nuclear experiments (A CMOS time to digital converter VLSI for high-energy physics). The schematic of TDC is depicted in Figure 2.2, in which the input propagates through a chain of digital buffers whose outputs are then fed into an array of D flip-flops while the stop signal latches the states of these flip-flops. Therefore, the output of flip-flops provides a thermometric representation which is time duration between input start signal and stop pulse.

Similar to ADCs, TDCs can also be categorized into Nyquist rate TDCs as well as oversampled noise shaping TDCs. Successive approximation (SAR) TDC has been addressed in [22] and pipeline TDC was proposed in [23]. Various configurations, which have been defined for ADC, can be defined for TDCs, as well. For example a two-step TDC has been proposed in [24]. In this topology the residual of the first stage is extracted and then is fed to the second stage for further process. The outputs of two-steps are digitally combined to form the overall output. Oversampled noise shaping TDCs have been widely used in time-of-flight (TOF) applications, positron emission tomography (PET), and all-digital phase-locked loops (ADPLLs) and etc. This type of data converter is also known as VCO-based quantizer in which the VCO acts as voltage to time converter and time information is then quantized by a bunch of counters. This class of data converter also has several members such as gated ring oscillator (GRO) [25], switched ring oscillator (SRO) [26], gated switched ring oscillator (GSRO) [27], VCO gated ring oscillator (VC-GRO) [28] and each of them has its own features, pros and cons. To conduct this research in a right path, three main categories have been investigated. 1) Nyquist rate TDCs used inside the loop filter of a delta sigma modulator. 2) VCO-based quantizer and its families as a standalone ADC/TDC, this category is referred to ring oscillator based data converter in *section 2.2.1.* 3) VCO-based quantizer used inside the loop filter of a delta sigma modulator.

Delta sigma modulators with embedded Nyquist rate TDCs

The use of amplitude-based quantizer such as FLASH, SAR or any other Nyquist rate ADC in a delta sigma loop filter is a design challenge thanks to voltage headroom limitations in advanced node technologies. Time/frequency coding instead of amplitude coding is an alternative to implement the quantizer inside the delta sigma loop filter. The most momen-

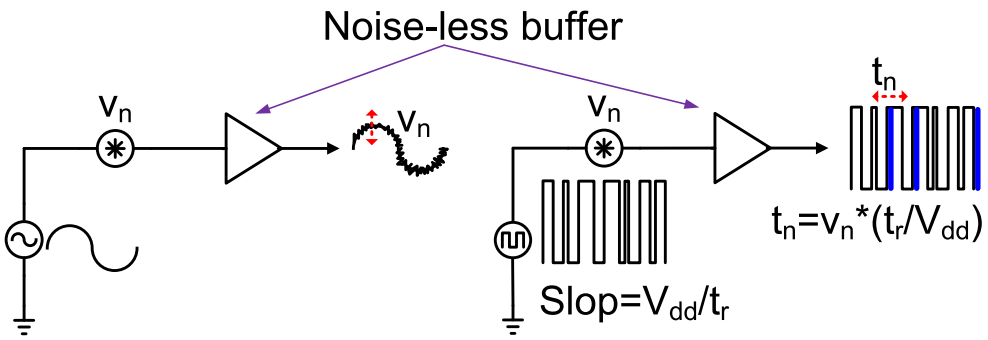


Figure 2.1 Translation of voltage noise to timing noise[21] (©[2011] IEEE)

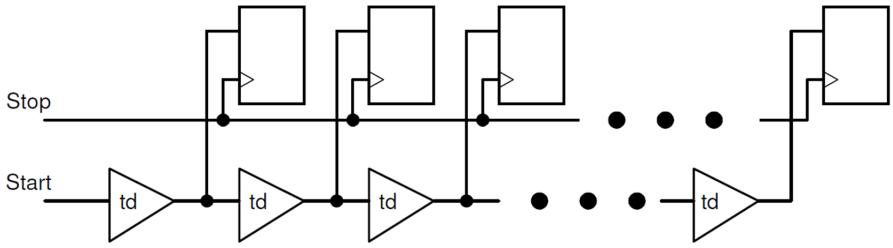


Figure 2.2 Basic single-shot TDC [21] (©[2011] IEEE)

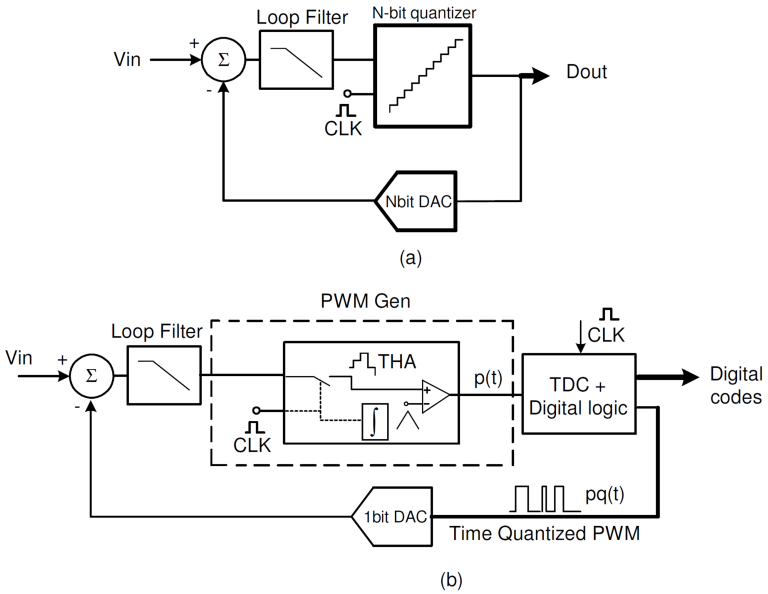


Figure 2.3 (a) Conventional multi-bit delta sigma modulator.(b) Time-domain quantizer/DAC based delta sigma modulator [21] (©[2011] IEEE)

tous advantage of this realization is that this technique is well-suited for sub-micron CMOS processes with low supply voltage. However, timing errors must be carefully scrutinized in

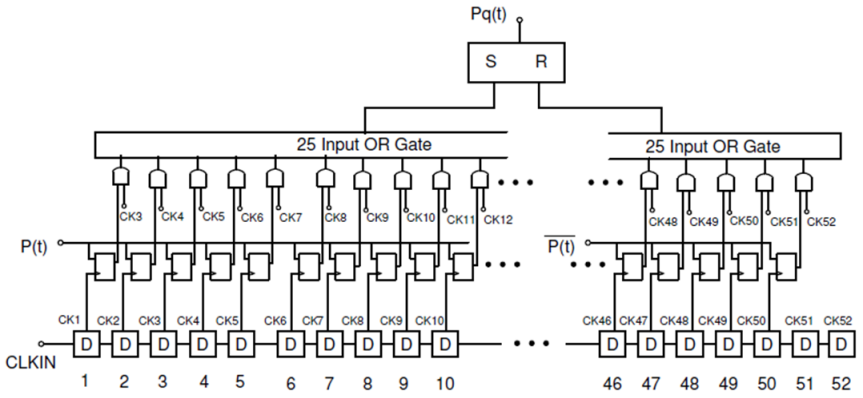


Figure 2.4 Simplified schematics of the TDC used as quantizer in a CT-DSM [21] (©[2011] IEEE)

this scenario. A CT-ΔΣM based on a time encoding quantizer (TEQ) has been addressed in [29]. This modulator shows the performance of the multi-bit CT-ΔΣM while the complexity is similar to single bit CT-ΔΣM by replacing the FLASH quantizer, DAC and its mismatch correction circuitries with TEQ similar to PWM modulator to reduce the silicon area at the expense of faster clock in the TEQ. A multi-bit CT-ΔΣM using time domain quantizer and feedback element has been proposed in [21]. Figure 2.3 shows the conventional multi-bit CT-ΔΣM along with the modulator proposed in [21]. In this architecture, the PWM-generator followed by TDC replaces the multi-bit quantizer and multi-bit DAC. The PWM block converts the voltage information to a pulse stream whose width is proportional to the amplitude of its input signal for every clock period. Digital codes at the output of the TDC correspond to the time edges of its input and it generates time-quantized feedback pulse, as well. Noise shaping is performed by a third order quasi-inverse-Chebyshev filter while both quantization noise of the TDC and non-linearity error of the PWM generator are noise-shaped. 1-bit DAC is used to provide feedback current pulse the time quantized digital waveform. The TDC used as a quantizer has been designed to generate 50 quantization steps in 4 nS period and the simplified schematic of the TDC is depicted in Figure 2.4 in which 50 clock phases are generated by a chain of inverters. Each phase is then used to drive the clock input of a flip-flop. The first 25 flip-flops are driven by PWM output pulse and the rest of 25 flip-flops are driven by complement of the PWM output pulse and OR-gate is in charge of accommodation of 25 inputs. Designed in 65 nm CMOS process, this architecture showed the $SNDR$ of 60 dB over 20 MHz signal bandwidth while output rate is 250 MSPS.

Standalone ring oscillator based data converters

As mentioned in the previous chapter, design of an ADC in deep sub-micrometer CMOS processes is a challenging task due to low supply voltage as well as technology scaling. However,

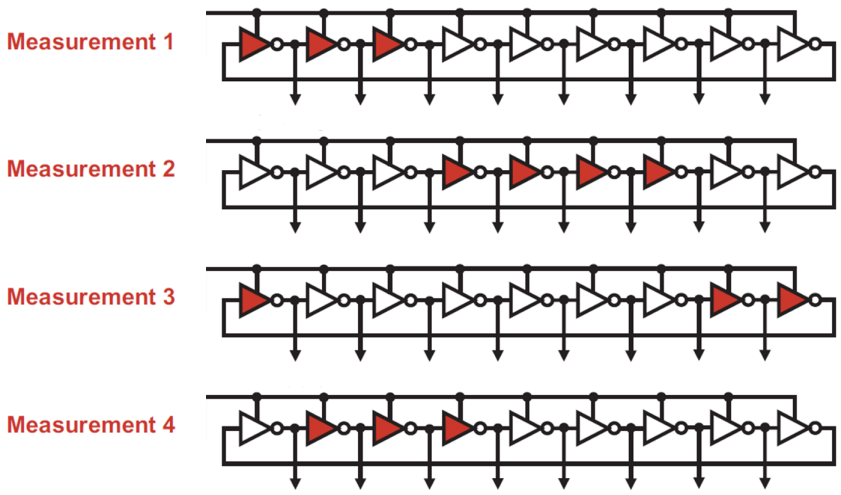


Figure 2.5 Barrel shifting occurs through delay elements across different measurements [30, 31] (©[2008] IEEE, ©[2009] IEEE)

for time domain circuits, time resolution is enhanced from the reduced transition of digital signals, which is in sort of tens of picoseconds in 90 nm CMOS and below. In a VCO-based ADC, input voltage is translated to a time-based signal whose frequency is proportional to the analog input. The frequency is then quantized by counting the edge of the VCO's output during the sampling period [30, 31]. Since the VCO produces a continuous phase output, the quantization noise of the previous sample affects that of current sample and hence and inherent first order noise shaping property can be obtained. Another important feature of a VCO-based ADC is that this topology consists of a ring oscillator followed by digital circuits. Therefore, sample rate of this architecture could be up to gigasamples per second in advanced node CMOS processes. VCO-based ADC also offers an appealing feature which is inherent dynamic element matching. As depicted in Figure 2.5, the VCO-based quantizer dynamically shuffles through delay stages in a barrel shift fashion as the measurement of edges in each reference period progress. Therefore, if the frequency is output variable of the quantizer, mismatch in delay across the stages is effectively first order noise shaped [30][31]. This feature is very important especially in the case of embedding a VCO-based quantizer inside the loop filter of a $\Delta\Sigma$M. The reason is that such a barrel shifting pattern and the resulting noise shaping is identical to the output pattern of the data weighted averaging (DWA) DEM algorithm. Therefore there is no need to implement an explicit DEM at the feedback path of the $\Delta\Sigma$M.

Due to mentioned unique features of the VCO-based quantizer, there has been a mass of research on it. Some publications have addressed a comprehensive analyses on VCO, techniques

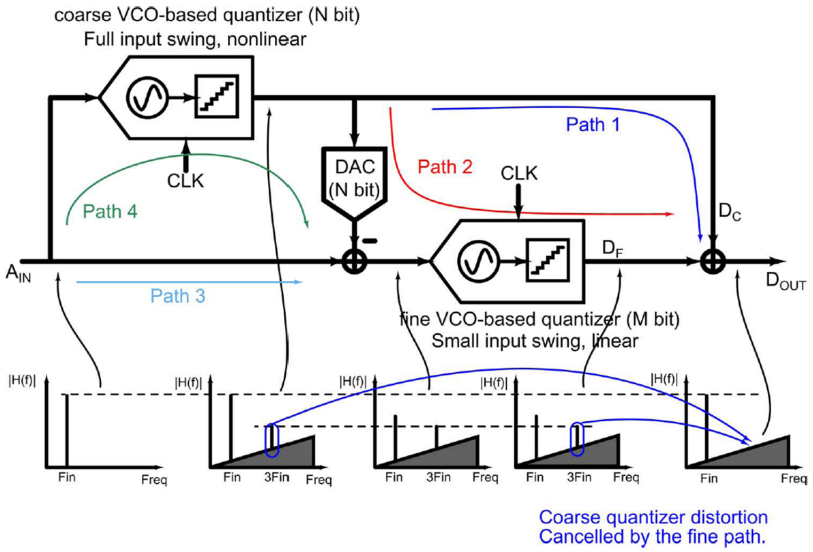


Figure 2.6 Two-step VCO-based delta sigma ADC architecture [32] (©[2015] IEEE)

to mitigate its voltage-to-frequency non-linearity [32, 33], other papers have introduces some applications [33–35], and the other have embedded the VCO-based quantizer inside the loop filter of a ΔΣM [30, 31, 13]. Although the latter is a technique to mitigate the non-linearity issue of a VCO-based quantizer, we are going to be investigating them in a separate section due to its importance. A comprehensive analysis of a VCO-based quantizer was published in [33] in which jitter, nonlinearity, mismatch, and the metastability of D flip-flops have been investigated. A two-step VCO-based delta sigma ADC has been introduced in [32, 36] in which a coarse VCO-based ADC digitizes the analog input signal while generation the nonlinearity. Then the quantization error is extracted and then the second VCO-based ADC digitizes the residue. Two outputs are summed up to generate the overall output. Two techniques are used in this structure. First, the severe non-linearity of the coarse VCO-based ADC is noise shaped by the fine VCO-based ADC. Second, the fine VCO-based ADC does not suffer from non-linearity since it is fed by a low swing analog signal. This architecture is shown in Figure 2.6. Fabricated in 40 nm CMOS process, the proposed two-step VCO-based ADC [32] shows the $SNDR$ of 59.5 dB over the bandwidth of 40 MHz with the sampling frequency of 1.6 GHz. A 0-2 MASH VCO-based ΔΣM has been recently reported in [37], based on traditional MASH 0-2 structures [38, 39], as illustrated in Figure 2.7. Unlike the traditional 0-2 MASH structure, which uses Nyquist rate ADCs to implement the first stage, a VCO-based ADC which offers a first order noise shaping was used to implement the first stage [37]. Therefore noise leakage due to imperfect matching will be first-order shaped. But the first stage does not provide any further noise shaping and that is why this architecture

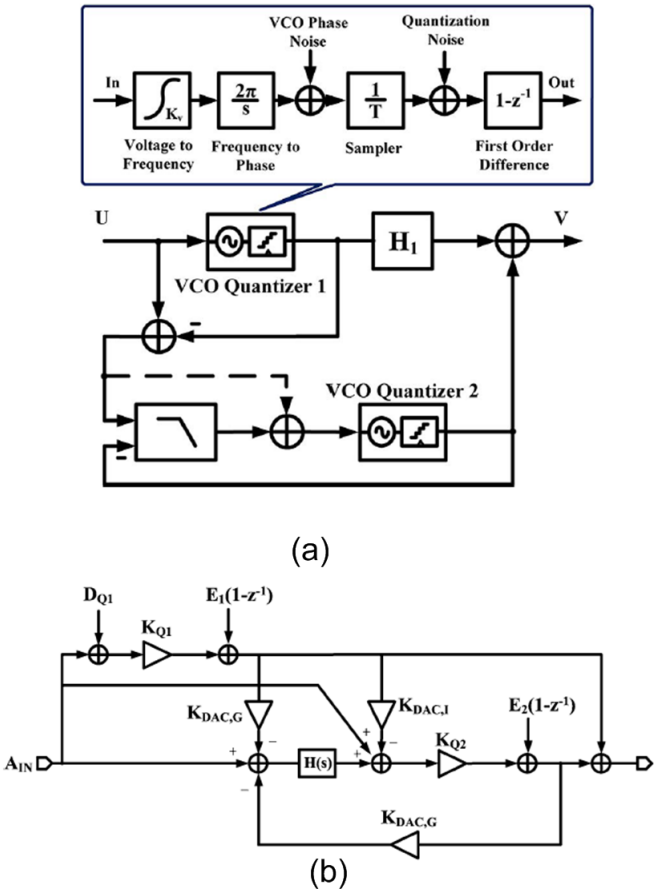


Figure 2.7 (a) Block diagram of a VCO-based 0-delta sigma MASH ADC, (b) Signal model of the proposed MASH ADC [37] (©[2015] IEEE)

was called MASH 0-2. The same method as presented in [32] was used to tackle non-linearity problem and the second stage just process the noise shaped quantization noise hence input voltage swing is greatly reduced. Regarding the signal model, shown in Figure 2.7(b), where $E_{1,2}$ are quantization noise of the first and second stage respectively. $K_{Q1,2}$ are the gain of the quantizers. $K_{DAC/G3}$ represents the gain of DACs and finally $H(s)$ is the $\Delta\Sigma$M loop filter. Under perfect matching, E_1 and D_{Q1} are fully cancelled and quantization noise of the second stage is noise shaped by $H(s)$. It should be mentioned that similar idea was proposed in [40] but no silicon was reported.

By taking the advantage of PWM signal, a highly linear VCO-Based ADC has been proposed in [41]. In this architecture, the analog voltage is first converted into a 2-level PWM signal using a naturally sampled PWM generator. The output of the PWM generator drives the VCO hence VCO operates at two frequencies i.e. f_{high} and f_{low} resulting linear operation of the VCO since just two operation points on the voltage-to-frequency transfer characteristic

are selected. We can conclude that the linearity problem moved back to the PWM generator. Fortunately, PWM generator can be made more linear than VCO. Moreover, the harmonics of carrier frequency of the PWM are located outside the signal bandwidth and can be removed by digital decimation filter. This architecture is illustrated in Figure 2.8. Using similar technique, a MASH 1-1 VCO-based ADC was proposed in [42], as shown in Figure 2.9. Unlike the architecture proposed in [41], a high-performance asynchronous delta sigma modulator ($A\Delta\Sigma M$) was utilized to generate PWM signal. The PWM signal is then controls the VCO. Quantization noise of the first stage is extracted using an array of phase detectors and the resulting error is applied to the second stage. Since the first VCO operates at two operation points it has linear performance. For the second VCO, the input signal is a low-swing analog signal and it shows linear performance as well. By proper selecting the carrier frequency of the A$\Delta\Sigma$M, harmonic distortion can be located outside the desired bandwidth.

Ring oscillator based ADC has other members such GRO, SRO, GSRO and VC-GRO. Getting started with the GRO paves the way to understand the rest of the structures. The concept of GRO was first proposed in 1997 and then it was extended and analyzed in 2009 [25]. The structure of GRO is illustrated in Figure 2.10, which shows the key concept of GRO. It's operation as simple as oscillation when the power supply is on and freezing its phases whenever the power supply is switched off. Similar to the VCO-based quantizer, the residue occurring at the end of a given measurement pulse can be transferred to the next measurement interval. This makes this architecture operate as a first order noise shaping quantizer like its first generation i.e. VCO-based quantizer. Numerous papers have been published just reporting either standalone GRO-based quantizers or its application in the PLLs or ADPLLs [43–46]. GRO-based MASH 1-1 topology has also been addressed in [47–49]. Based on the concept of the GRO , time-domain error feedback filter and MASH structure, a fourth order delta sigma time to digital converter has been addressed in [50]. The configuration is shown in Figure 2.11. The first stage is a standalone GRO-based TDC that presents first order noise shaping. Quantization error of the first stage, which is the time domain, is then extracted to feed to the second stage. Second stage of this architecture is a third order delta sigma TDC. This stage consists of a GRO-TDC as a core while the quantization error, which is aslo represented in the time domain, is extracted. Instead of using conventional integrator, a time domain error feedback, as shown in Figure 2.11, is used to provide extra 2^{nd} order noise shaping. The architecture proposed in [50] offers a fully time domain delta sigma TDC.

Regarding the ring-oscillator based ADCs, have been reviewed up to now, there are noticeable issues which are itemized here. 1) Performance of the VCO-based ADC is limited by the non-linear voltage-to-frequency transfer characteristic of the VCO but its unique features such as first order noise shaping and inherent dynamic element matching is alluring and irreplaceable.

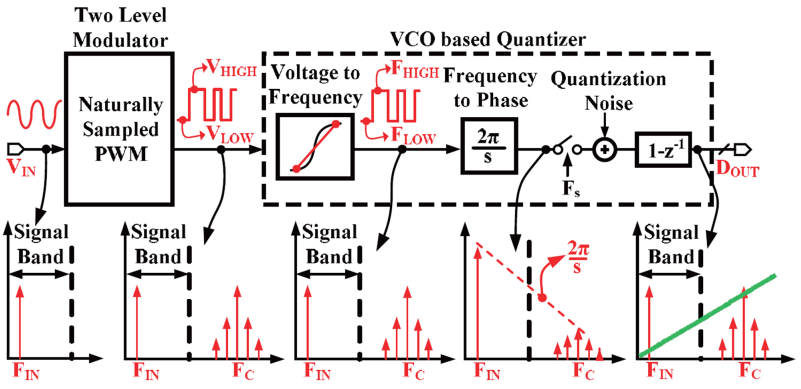


Figure 2.8 PWM-generator followed by VCO-based ADC [41] (©[2011] IEEE)

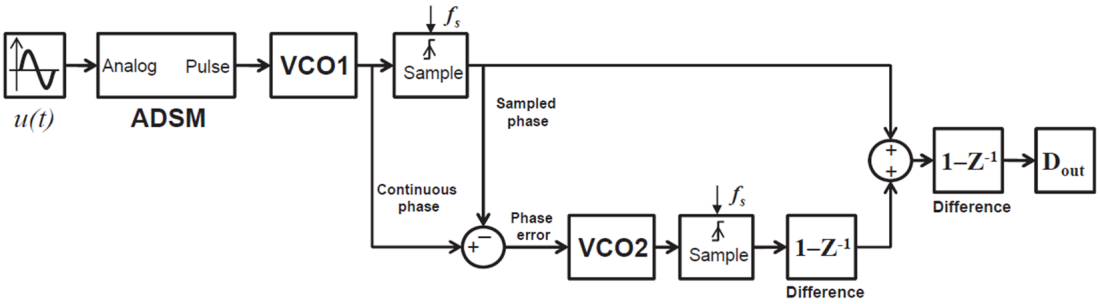


Figure 2.9 PWM-generator followed by VCO-based ADC [42] (©[2012] IEEE)

2) Two-step VCO-based ADC could resolve this problem to some extend but the VCO-based ADC located in the first stage is still experiencing full input swing, resulting nonlinearity. 3) In the case of VCO-based ADC controlled by PWM signal or even in the case of GRO-TDC, although the VCO or GRO behaves linearly, in fact the non-linearity property moved back to the PWM block. However, PWM generator can be designed with superior linearity. 4) Open loop MASH 1-1 structures are quite sensitive to the delay of quantization error generator.

Delta sigma modulators with embedded VCO-based quantizer

As mentioned in the previous section, the performance of the VCO-based quantizer is severely limited by nonlinearity of the VCO's voltage-to-frequency transfer characteristic since increasing the signal power makes the VCO exercise the entire non-linear range. Therefore, severe distortion appears at the output of the VCO-based ADC. To simultaneously suppress the VCO nonlinearity and increase the order of noise shaping the VCO-based ADC was embedded inside the ΔΣM's feedback loop as a first order noise shaping quantizer, as illustrated in Figure 2.12 [30, 31].

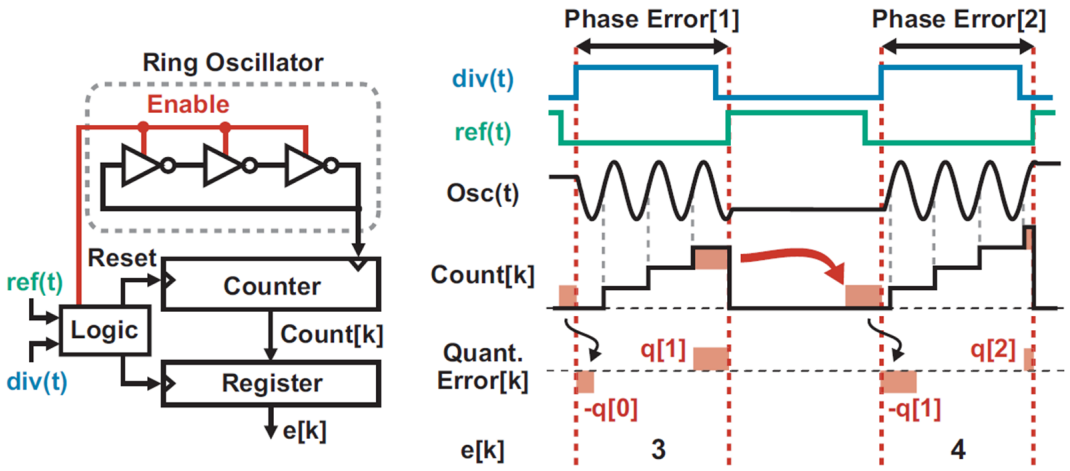


Figure 2.10 Gated ring oscillator TDC [25] (©[2009] IEEE)

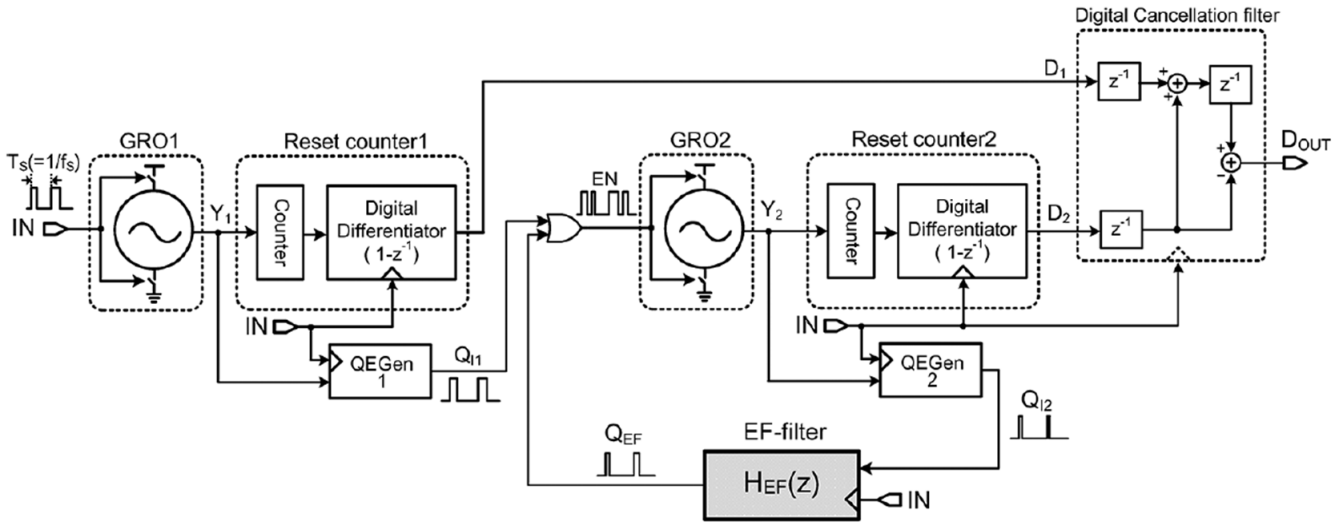


Figure 2.11 GRO-based MASH 1-3 and its timing error feedback filter [50] (©[2015] IEEE)

In this topology, loop filter ($L(s)$) suppresses the VCO nonlinearity to extend its $SNDR$. It is apparent that the higher order loop filter, the better non-linearity suppression and as a consequence the better performance in terms of $SNDR$. This also means that the effectiveness of this technique greatly depends on the gain of the loop filter. The VCO-based ADC's input spans the entire signal range and therefore it exercises the entire nonlinear tuning curve of the VCO. That is why high gain loop filter is needed to suppress the large amount of distortion caused by the VCO. For example, for a fixed OSR of 32, a standalone 31-level VCO-based quantizer presents 62 dB $SNDR$ while the $SFDR$ is about 35 dB. Increasing the order of

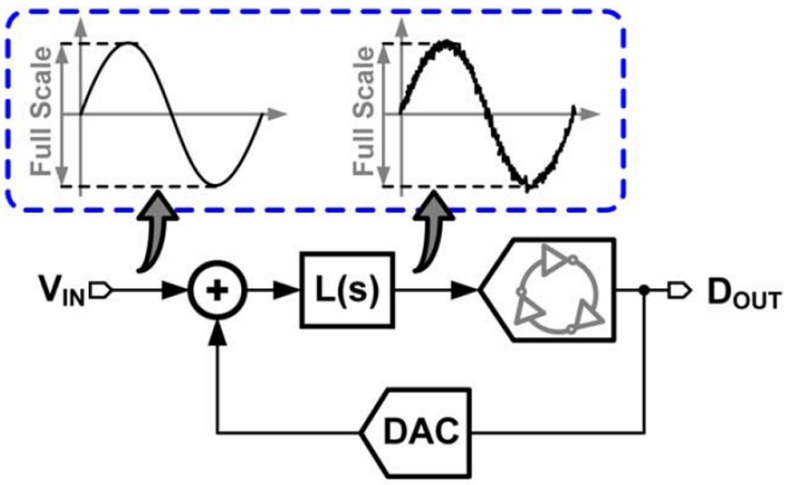


Figure 2.12 CT-ΔΣM with VCO-based quantizer [13, 30, 31] (©[2012] IEEE, ©[2008] IEEE, ©[2009] IEEE)

the loop filter results the $SNDR$ and $SFDR$ of 86 and 58 dB, respectively. Further analysis shows that at least third order loop filter is required to achieve an $SFDR$ of 88 dB. It is worth mentioning that third order loop filter along with first order quantizer results a forth order ΔΣM. Not only does such a higher order ΔΣM suffer from higher level of complexity and power consumption but it is also prone to instability. In the modulator proposed in [30], VCO output frequency was used for design variable since it has proportional relationship with the input signal. As a result, to exercise the full dynamic range of the VCO-based quantizer, the VCO input signal must span the entire the non-linear transfer characteristics. To avoid spanning this non-linear transfer characteristic, output phase of the VCO was used in [31] to form a fourth order CT-ΔΣM. Before reviewing the architecture proposed in [31], it is worth spending more time on the voltage-to-phase VCO ADC. Figure 2.13 shows the block diagram of a voltage-to-phase VCO ADC. Here, the VCO phase is sampled and quantized by registers and a phase detector compares the registers output with the reference phase by employing a simple phase detector. The resulting signal is fed into the input of a DAC and resulting analog signal is subtracted from the input signal. The residue is then applied to the VCO and the VCO provides integration for the next cycle. Since the VCO serves as an integrator and a negative feedback is formed this architecture is actually a first order CT-ΔΣM. Both voltage-to-frequency VCO ADC and voltage-to-phase VCO ADC is modeled and simulated in *CPPSIM* simulator for 1GHz sampling frequency over 20 kHz signal bandwidth while the same non-linearity is considered for both case. It can be concluded from Figure 2.14 that in the case of voltage-to-frequency VCO ADD $SNDR$ is primarily limited by the distortion

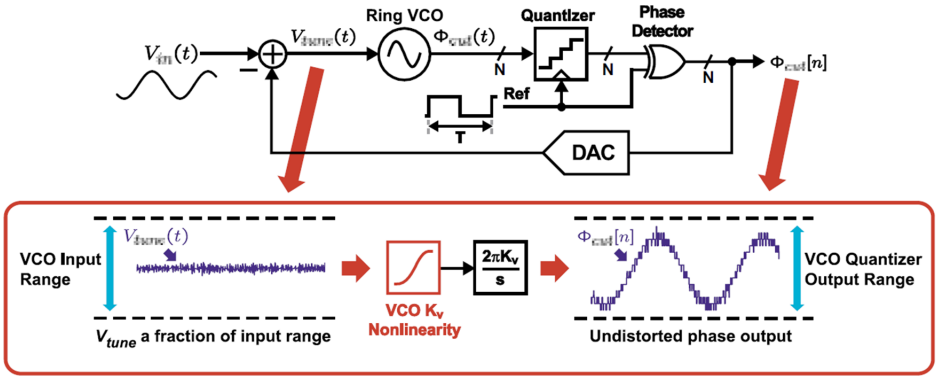


Figure 2.13 Voltage-to-phase VCO-based ADC [31] (©[2009] IEEE)

while in the case of voltage-to-phase VCO ADC the distortion tones are almost eliminated and provides 36 dB $SNDR$ improvement rather than the latter case. The voltage-to-phase VCO ADC [31] was employed inside a forth order ΔΣM to provide the $SQNR$ of about 95 dB over 20 MHz signal bandwidth, as shown in Figure 2.15. Cascade of integrators with feed forward distribution was used to lower the integrator output swings.

To avoid using higher order single loop modulator as well as getting rid of the nonlinearity problem of a VCO, a residue-cancelling VCO-based quantizer has been addressed in [13, 51] and it was employed in a first order CT-ΔΣM to form a second order CT-ΔΣM, as depicted in Figure 2.16. The idea behind the residue-cancelling VCO-based quantizer is to minimize the voltage swing at the input of the VCO. To do so, a FLASH ADC digitizes the input voltage signal while the output digital codes are converted back to the analog signal using a DAC and the resulting signal is subtracted from analog input signal. The residue, which is sitting down inside the linearity range of the VCO, is then control the VCO. The VCO based ADC digitizes this quantization error and finally the output of FLASH ADC and VCO-based ADC are combined to generate the output bit stream. It is worth noting that a similar architecture was proposed before in [52].

Another technique to circumvent the non-linearity problem of the VCO-based quantizer has been introduced in [53] in which the nonlinearity problem was resolved outside the loop filter instead of embedding it inside the loop filter of ΔΣM. The idea behind this modulator is that the first stage is a conventional first order SC-ΔΣM while the quantization noise of the first stage is extracted and the injected to a VCO-based quantizer. The outputs of two stages are added using a DCL hence a MASH 1-1 is formed. Since the input of the VCO is just a quantization error, the VCO does not exercise the whole non-linear range and therefore it operates almost linearly. Another main feature of this architecture is that the VCO-based

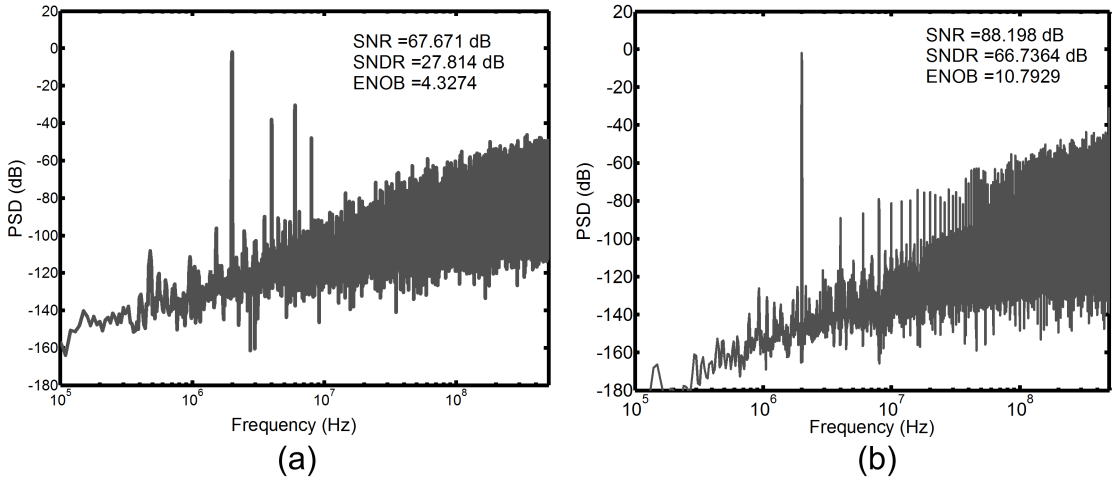


Figure 2.14 PSD of (a) voltage-to-frequency VCO ADC [30], (b) voltage-to-phase VCO ADC [31] (©[2008] IEEE, ©[2009] IEEE)

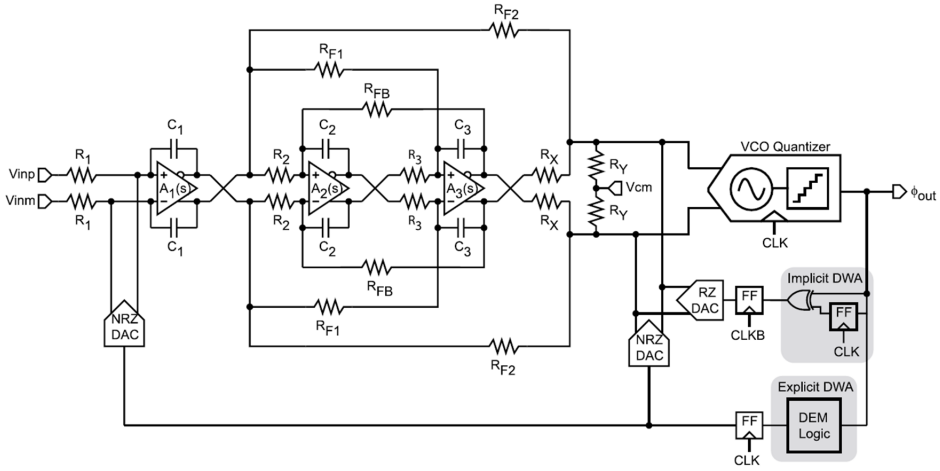


Figure 2.15 Fourth order CT-ΔΣM with voltage-to-phase VCO-based ADC [31] (©[2009] IEEE)

quantizer operates 12 times faster than the first stage. Therefore, not only does not the first stage suffer from stringent requirements on op-amp, but the $SNDR$ goes up similar to what occurs in a multi-rate ΔΣMs.

Having reviewed above four techniques to mitigate the non-linearity of the voltage-to-frequency transfer characteristic, there are several issues. First, embedding the voltage-to-frequency VCO-based quantizer inside the loop filter needs high-order modulator which is susceptible to instability and the power consumption of such architectures is not negligible. In the case of voltage-to-phase VCO ADC, although the nonlinearity problem is relatively improved, it

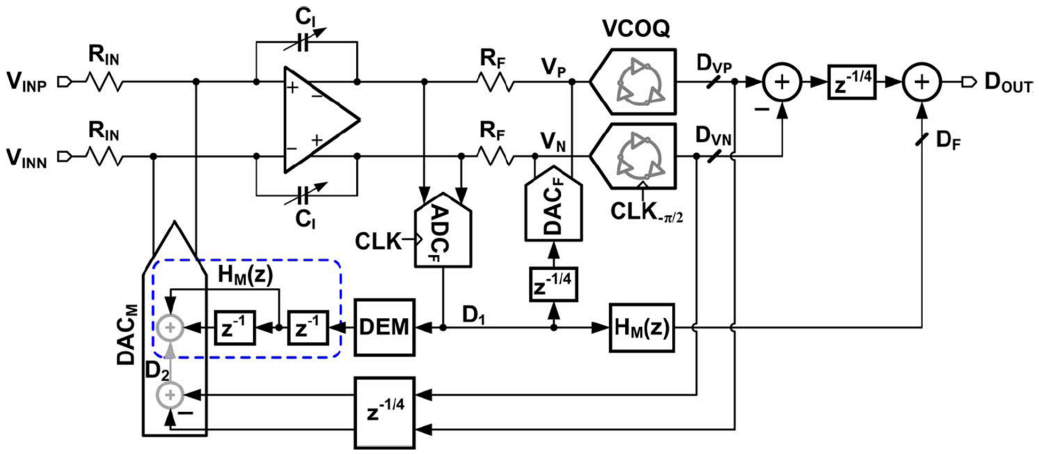


Figure 2.16 Second order CT-ΔΣM with residue-cancelling VCO-based quantizer [13] (©[2012] IEEE)

still needs a higher order modulator. Another problem is that this VCO-based ADC no longer offers an inherent dynamic element matching since there is not differentiator at the back-end of the VCO-based quantizer. In the case of residue cancelling VCO-based quantizer, FLASH ADC accompany with DAC and it error correction circuitry must be used to generate residue hence it costs silicon area as well as power consumption. And finally, in the case of multi-rate MASH structure followed by VCO-based quantizer there are two issues ; 1) This architecture is not potentially suitable for high band width application because of the technology limitation in SC-implementation. 2) Multi-bit quantizer must be used inside the loop of the first stage to reduce the quantization error and confine it in the linear range of the VCO-based quantizer.

2.3 Conclusion

Literature review has been performed on SC-ΔΣM to design a LBW SC-ΔΣM to cover 20 kHz signal bandwidth. It has been inferred that both system level optimization as well as circuit level techniques must be properly used to have a power optimized SC-ΔΣM. From the second part of the literature review, it has been concluded that CT-ΔΣM is the best option for high resolution high bandwidth application. To make the design suitable for advanced CMOS process with low supply voltage, part of the design can be implemented in the time domain. In doing so, Nyquist rate TDC as well as VCOQ have been used. Nyquist rate TDC does not offer any noise shaping while VCOQ offers this feature. It also has implicit DEM property. However, this class of ADC severely suffers from non-linearity.

CHAPTER 3 ARTICLE 1 : A 0.9-V 100-μW FEEDFORWARD ADDER-LESS INVERTER-BASED MASH $\Delta\Sigma$ MODULATOR WITH 91-dB DYNAMIC RANGE AND 20-kHz BANDWIDTH

3.1 Overview

As described in the previous sections, conventional FF topology suffers from a power hungry adder to sum up the feed forward branches. This issue is addressed in this chapter by moving back the adder to the input of the second integrator in the second order $\Delta\Sigma$M. The quantization error is extracted in the voltage domain and then fed into the back-end stage which is similar to the front-end stage. A self and body biased inverter-based OTA operating in the weak inversion is also proposed to overcome the issues related to the weak-inversion region. The following sections are the reproduction of an accepted article in IEEE Transactions on Circuits and Systems-I : Regular Papers

— Article 1 : M. Honarparvar, J. M. de la Rosa and M. Sawan, "A 0.9-V 100-μW Feedforward Adder-Less Inverter-Based MASH$\Delta\Sigma$Modulator With 91-dB Dynamic Range and 20-kHz Bandwidth," in IEEE Transactions on Circuits and Systems I : Regular Papers, vol. 65, no. 11, pp. 3675-3687, Nov. 2018 [54].

3.2 Abstract

A 0.9-V $\Delta\Sigma$ modulator integrated in a 0.18-μm CMOS technology for digitizing signals in low-power devices is presented in this paper. To do so, a cascade (MASH) architecture based on an *adder-less* feedforward structure is proposed. The proposed modulator has a unity signal transfer function in both stages of the modulator in order to reduce the integrators output swings. To mitigate the failure of slow process corner in the weak inversion as well as to further diminish the power consumption of the presented modulator, a fully differential self and bulk biased (SBB) inverter-based OTA is proposed. Experimental results are shown to demonstrate the efficiency of the proposed $\Delta\Sigma$ converter, showing state-of-the-art performance, by featuring 88.7-dB SNR, 86.4-dB SNDR and 91-dB DR within a signal bandwidth of 20-kHz, with a power dissipation of 103.4-μW when the circuit is clocked at 5.12-MHz.

Key Words : Analog-to-digital conversion, delta-sigma modulation, switched-capacitor circuits, inverter-based OTAs.

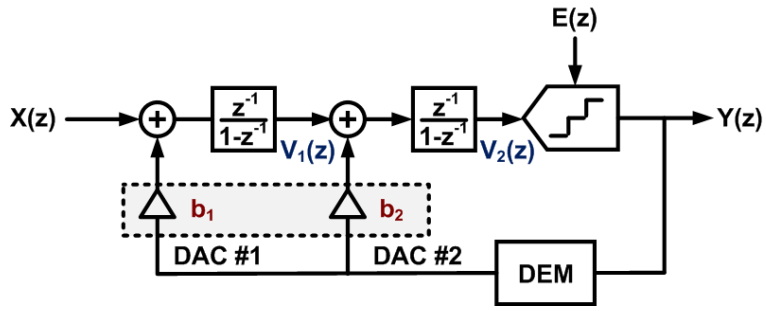
3.3 Introduction

The need for hand-held devices, smart-phones and medical implantable microelectronic systems, is remarkably growing up. However, keeping all these electronic devices power optimized is one of the main challenges due to the lack of life-time batteries utilized to power them up. One of the most critical building blocks of such devices is the analog-to-digital converter (ADC), since it needs to efficiently digitize acquired signals in a hostile environment. Compared to other ADC techniques, Delta-Sigma Modulators ($\Delta\Sigma$Ms) have been widely used in those devices due to the unique features they offer and they are capable of being effectively power optimized at both architectural and circuit levels [2]-[55]. Nevertheless, special care must be taken into account to optimize the performance of $\Delta\Sigma$Ms. Indeed, many state-of-the-art high-resolution (>14-bit) low-bandwidth (<25-kHz) $\Delta\Sigma$Ms have been reported, including single-stage architectures [56]-[5] and cascade topologies – also referred to as Multi stAge noiSe sHaping (MASH) [2]-[19]. Among other $\Delta\Sigma$ loop-filter topologies, the so-called feedforward (FF) structure has been successfully used by some designers to implement single-stage high-order (third-order or more) noise shaping [20]-[16]. However, the main limitation of FF structures is the power-hungry adder required at the input of the quantizer. This adder constitutes one of the main design bottlenecks of FF $\Delta\Sigma$Ms employed in ADCs, where the energy consumption becomes critical. In order to mitigate this limitation, some authors have proposed alternative implementations of the FF loop-filter. Thus, the $\Delta\Sigma$M reported in [20] includes a fourth-order FF loop-filter with a passive adder. However, this technique suffers from both reduction of signal swing at the input of the comparator, and mismatch between capacitors. A similar strategy has been adopted in [16], where a 1.5-bit (3-level), fourth-order FF structure is proposed for digitizing signals with a 20-kHz bandwidth. Another approach consists of using switch matrix feedback compensation based on a direct summation technique as proposed in [15]. While such technique is well-suited for multi-bit quantizers, it is not applicable to single-bit $\Delta\Sigma$Ms. Moreover, employing multi-bit quantizers in high-resolution applications is limited by the inherited nonlinearity of the DAC used in the feedback path of the $\Delta\Sigma$ modulator. This requires using linearization techniques, such as dynamic element matching (DEM), which obviously leads to increasing the circuit complexity as well as the power consumption. Similar FF topologies have been addressed in [57]-[58] where the last integrator serves as an integrator and an adder simultaneously. However, an extra DAC in the feedback path is needed to retrieve the noise transfer function (NTF) of the modulator. It is worth noting that in all above-mentioned topologies, an extra DAC is required to extract the quantization noise if they are supposed to be used in a MASH configuration and hence adds circuit complexity.

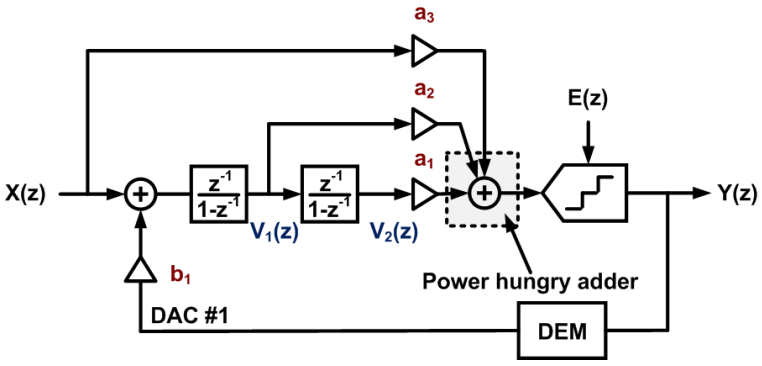
Apart from the strategies to optimize the performance of ΔΣMs at system level, an important effort should be put also at circuit level. Scaling of CMOS technologies brings significant improvements in terms of functionality, speed, size, form factor and power consumption–to the digital circuits. However, such an aggressive process scaling comes along with the reduced supply voltage to ensure the proper functionality of the device and reduces the intrinsic gain of CMOS transistors. The mentioned constraints make the design of the analog building blocks, e.g. operational transconductance amplifiers (OTAs), in a ΔΣ converter very challenging such that it limits the application of the traditional OTA topologies [59]. On the other hand, a lower supply voltage reduces the voltage headroom and the available signal swing. This results in the dynamic range being limited by thermal noise. It also confines the choice of circuit architectures. Besides the mentioned drawbacks, biasing a circuit in the weak inversion, to minimize the power dissipation, is still of interest. However, such a biasing region makes the circuit severely susceptible to the process variations due to fluctuations in MOS parameters and it may decay the performance of a complex system like ΔΣ converters. Having discussed from that point of view, not only is an appropriate OTA topology needed, but proper remedy must be taken when biasing the OTA in the weak inversion [60].

This paper contributes to improve the performance of FF ΔΣMs by exploring two approaches at the architectural and circuit levels, in order to mitigate the mentioned problems to realize a high-efficiency, high-resolution ΔΣM, which covers the audio band (20-kHz) in a sub-1V environment using a 0.18-μm CMOS technology. To this end, a fourth-order *adder-less* MASH ΔΣM operating at 0.9-V is presented in this work as an extension and improved version of the paper presented by the authors in [59]. Although the alternative sturdy MASH structure based on the adder-less FF loop-filter, proposed in [61], relaxes the OTA DC-gain requirement, it will be shown that only a DC-gain of 50 dB is sufficient for the proposed MASH structure. Therefore, the main focus of this work at the circuit level is to keep the OTA structure as simple as possible and power efficient. A fully differential SBB inverter-based OTA, operating in the weak inversion, is therefore proposed to implement the integrators of the proposed ΔΣM. It is shown that the proposed OTA is robust against slow corners and low supply voltage.

The paper is organized as follows. Section 3.4 provides a background on the feedback and feedforward ΔΣMs. Section 3.5 describes the proposed ΔΣM architecture and some system-level design considerations. High-level synthesis, analysis and optimization are addressed in Section 3.6. Section 3.7 demonstrates the circuit level implementation of the proposed ΔΣM including SBB inverter-based OTA, switches and comparator. Experimental results are given in Section 3.8 and finally a conclusion is drawn in Section 3.9.



(a)



(b)

Figure 3.1 Conventional ΔΣM architectures (a) FB structure, (b) FF structure.

3.4 Background on Feedback and Feedforward ΔΣMs

As can be seen in Fig. 3.1, there are two main architectures to implement a ΔΣM, namely : (1) Feedback (FB) topology and (2) FeedForward (FF) topology [4]. Usually, FF ΔΣMs are preferred because they present lower integrators output swings and less feedback DACs than their FB counterparts. However, FF topology requires a power-hungry adder placed before the quantizer [56] and out-of-band peaking in the signal transfer function (STF) [20]. If we simply consider a second-order FB structure ($b_1 = 1$, $b_2 = 2$) and a linear model of the quantizer, the output of a second-order ΔΣM can be expressed as follows :

$$Y_{FB}(z) = z^{-2} \cdot X(z) + (1 - z^{-1})^2 \cdot E(z) \tag{3.1}$$

In which $X(z)$, $Y_{FB}(z)$ and $E(z)$ are the input, output and quantization noise of the modulator, respectively. Therefore, the modulator shows a STF of z^{-2} and and noise transfer function (NTF) of $(1-z^{-1})^2$. Analyzing the output of the integrators – shown in Equations 3.2 and 3.3 – it can be shown that the integrators process the input signal.

$$V_1(z) = z^{-1} \cdot (1 + z^{-1}) \cdot X(z) - z^{-1} \cdot (1 - z^{-1}) \cdot E(z) \tag{3.2}$$

$$V_2(z) = z^{-2} \cdot X(z) - z^{-1} \cdot (2 - z^{-1}) \cdot E(z) \tag{3.3}$$

The obvious consequence of this dependency is that the output swing of the amplifier must be large enough, which makes the design of the amplifier in low voltage environment more troublesome. Moreover, the harmonics generated by the amplifier's non-linearity, which depends on the integrators swing, drastically degrades the performance of the $\Delta\Sigma$M in terms of the Signal-to-(Noise+Distortion) Ratio (SNDR). Alternatively, the output of the second-order FF $\Delta\Sigma$M in Fig. 3.1 ($a_1 = 1$, $a_2 = 2$, $a_3 = 1$, $b_1 = 1$) can be expressed as follows in the Z-domain :

$$Y_{FF}(z) = X(z) + (1 - z^{-1})^2 \cdot E(z) \tag{3.4}$$

where the FF topology shows a STF of 1 (unity STF) and an NTF of $(1 - z^{-1})^2$. Moreover, the integrators output are expressed as follow :

$$V_1(z) = -z^{-1} \cdot (1 - z^{-1}) \cdot E(z) \tag{3.5}$$

$$V_2(z) = -z^{-2} \cdot E(z) \tag{3.6}$$

Note that expressions 3.5 and 3.6 show the integrators process the quantization noise only, which means that the signal swing at the output of integrators are smaller than their FB counterparts and, as a result, the distortion generated by the non-linearity of the amplifier is not noteworthy. In addition, the implementation of the amplifier is easier since signal amplitude of the amplifier is reduced. Therefore, it can be inferred that FF architecture is a well-suited topology to implement low-voltage low-power $\Delta\Sigma$Ms. However, the most momentous bottleneck of the FF structure is the adder before the quantizer, which could be realized either using active or passive circuits. Although active adder, which presents an accurate summation, is more reliable, a fast power hungry OTA needs to be realized to incorporate into the active adder. Alternatively, a passive adder can be used. Although such a technique is well-suited for low power applications, signal swings and the quantizer input step are degraded due to the parasitics [56]. In addition, the quantizer kick-back noise as well as capacitor mismatches may severely degrade the overall SNDR of the modulator. Finally, the area occupied by passive circuit elements may impose a severe restrictions [62].

3.5 Proposed Adder-less MASH FF ΔΣM

As mentioned in the introduction, FF ΔΣM is a well-suited topology to implement low-voltage low-power ΔΣMs. However, the key bottleneck of the FF structure is the adder before the quantizer, which could be realized either using active or passive circuits. Although an active adder, which allows for an accurate summation, is more reliable, a fast power-hungry OTA needs to be realized in order to incorporate into the active adder. Alternatively, a passive adder can be used. Although such technique is well-suited for low-power applications, signal swings and the quantizer input step are degraded due to the parasitics [56]. In addition, the quantizer kick-back noise as well as capacitor mismatches may severely degrade the overall signal to noise plus distortion ratio (SNDR) of the modulator. Finally, the area occupied by passive circuit elements may impose significant restrictions [62].

3.5.1 Adder-less Single-stage Feedforward Architecture

Dynamic Behavior of the Adder-less ΔΣM

The approach to overcome the aforementioned problem is to perform the signal summation at the input of the last integrator instead of the quantizer input, as depicted in Fig. 3.2. In other words, the last integrator is shared to serve as an integrator and as an adder simultaneously. Consequently, both the circuit complexity and the power consumption can be reduced. Without loss of generality, all coefficients are assumed to be set to unity in Fig. 3.2, i.e. $b_1 = 1$ and $a_i = 1$, $i = 1, 2, 3, 4$. In this case, the NTF and STF of the modulator can thus be respectively written as follows :

$$NTF(z) = \frac{(1 - z^{-1})}{(1 - z^{-1}) + z^{-1} \cdot I_2(z) \cdot (1 + G(z))} \tag{3.7}$$

$$STF(z) = \frac{z^{-1} \cdot I_2(z) \cdot (1 + G(z)) + H(z) \cdot I_2(z)}{(1 - z^{-1}) + z^{-1} \cdot I_2(z) \cdot (1 + G(z))} \tag{3.8}$$

Comparing (1) and (2) to that of the conventional second order FF structure with an $NTF(z) = (1 - z^{-1})^2$, $I_2(z)$, $G(z)$ and $H(z)$, as depicted in Fig. 3.2, are considered to have a second-order noise shaping as well as a unity STF as follows. It is worth noting that any arbitrary NTF can be mapped onto the ΔΣM in Fig. 3.2, resulting in different coefficient values.

$$I_2(z) = \frac{1}{(1 - z^{-1})} \tag{3.9}$$

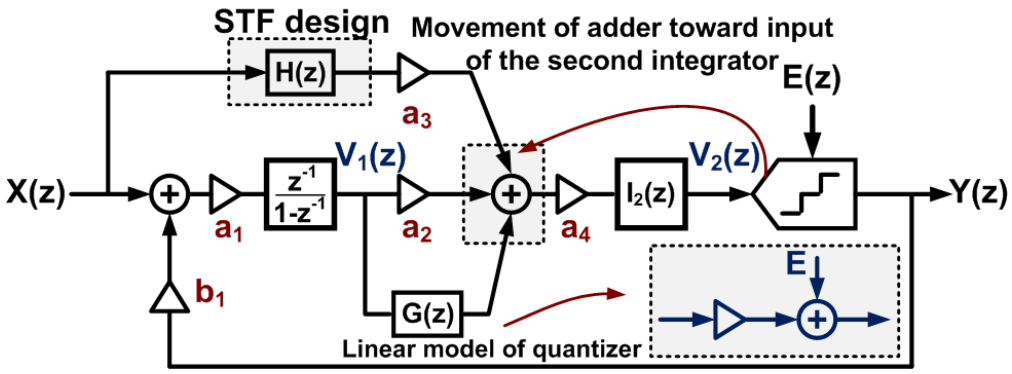


Figure 3.2 Adder-less FF ΔΣM with single (multi)-bit quantizer.

$$G(z) = H(z) = 1 - z^{-1} \tag{3.10}$$

It is valuable to write the integrator outputs for the adder-less modulator, depicted in Fig. 3.2. As can be seen from (5) and (6), the first integrator processes the quantization noise while the output of the second integrator includes the input signal component. Note that any non-idealities caused by the second-order integrator are shaped by the loop-filter, so that these non-idealities do not severely influence the performance of the modulator.

$$V_1(z) = -z^{-1} \cdot (1 - z^{-1}) \cdot E(z) \tag{3.11}$$

$$V_2(z) = X(z) - z^{-1} \cdot (1 - z^{-1}) \cdot E(z) \tag{3.12}$$

Quantization Error Extraction of the Adder-less ΔΣM

The conventional method to extract the quantization error in a MASH ΔΣM is to subtract the quantizer output from the quantizer input, as shown in Fig. 3.3. However, such an approach exacerbates the complexity of the quantization error extraction, especially when the number of quantizer level increases. This is due to the fact that the quantizer output is represented in thermometer code and a multi-bit switched capacitor (SC)-DAC is needed to perform such a subtraction.

As shown in [63], [64], a delayed version of the quantization error is available at the output of the second integrator in the FF topology, which makes this topology desirable for a MASH structure as well as for extended counting incremental ADCs. However, this is not the case in the proposed ΔΣM since the quantization error is high-pass filtered at the output of the first integrator and the second integrator processes both the input signal and the quantization

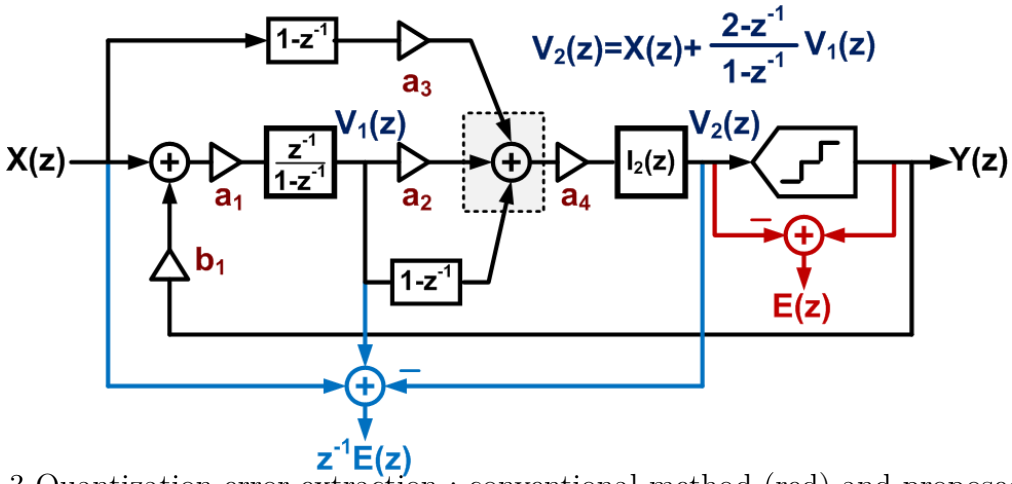


Figure 3.3 Quantization error extraction : conventional method (red) and proposed method used in the adder-less FF ΔΣM (blue).

error as well. Fortunately, the quantization error is available in the proposed architecture if the signals at different nodes of the modulator are properly traced. Setting all coefficients at unity- to simplify the analysis- results in a second-order NTF i.e. $NTF(z) = (1 - z^{-1})^2$ and the output of the second integrator, $V_2(z)$, can be expressed as a function of input signal, $X(z)$, and first integrator output, $V_1(z)$ as follows :

$$V_2(z) = X(z) + \frac{2 - z^{-1}}{1 - z^{-1}} \cdot V_1(z) \tag{3.13}$$

Substituting (5) and (7) in expression (8) shows that with proper combination of the input signal of the modulator, $X(z)$, and the output of the first and second integrators ($V_1(z)$ and $V_2(z)$), a delayed version of the quantization error can be extracted in the adder-less FF topology, yielding :

$$X(z) + V_1(z) - V_2(z) = z^{-1} \cdot E_1(z) \tag{3.14}$$

where $E_1(z)$ is the quantization error of the front-end stage.

3.5.2 Proposed Adder-less MASH Feedforward Architecture

In order to ensure a high performance power optimized ΔΣM, its system-level parameters, i.e. the order of the loop-filter, the OSR and the number of bits of the embedded quantizer, must be carefully determined. Moreover, the selection between a single-stage and a MASH structure is another important decision to make. Increasing the quantizer resolution leads to increasing the SNDR of the modulator at the expense of circuit complexity and power

consumption. Moreover, linearization techniques are required to suppress nonlinear behavior of the feedback DAC. To get rid of these problems, a single-bit quantizer is considered in this design.

Although a higher SNDR can be achieved with a higher order modulator, it makes the modulator susceptible to instability. Single-bit quantizer even exacerbates the stability issue. Alternatively, a MASH $\Delta\Sigma$M is a suitable solution in which the order of the modulator can be increased by cascading low-order (typically first-order and second-order) stages, which are inherently stable, and hence the overall $\Delta\Sigma$M structure is stable [4]. Based on these considerations, a MASH $\Delta\Sigma$M with single-bit quantizer is chosen in this work.

In order to determine the OSR and the order of the modulator, an extensive analysis, fine tuned by behavioral simulation, is carried out to maximize the SNDR of the $\Delta\Sigma$M with the minimum power consumption. As depicted in Fig. 3.4, a fourth-order MASH structure $\Delta\Sigma$M (MASH 2-2), which consists of the two stages second-order adder-less $\Delta\Sigma$Ms with a single-bit quantizer, is considered for this design. Note that the quantization error is extracted as described in the previous section and the explicit adder at the input of the second stage is for illustrative purposes only. In a practical implementation, all signals are summed up at the input of the third and fourth integrators, as will be detailed in Section 3.7. An OSR of 128 with the sampling frequency of 5.12 MHz is selected to make the proposed modulator operate over a 20-kHz signal bandwidth.

Assuming the NTF of $(1 - z^{-1})^2$ for each stage of the proposed $\Delta\Sigma$M, the output of the first and second stage can be respectively expressed as :

$$Y_1(z) = X(z) + (1 - z^{-1})^2 \cdot E_1(z) \tag{3.15}$$

$$Y_2(z) = z^{-1} \cdot E_1(z) + (1 - z^{-1})^2 \cdot E_2(z) \tag{3.16}$$

and the overall z-domain output signal of the proposed $\Delta\Sigma$M is given by :

$$Y_{Proposed-MASH}(z) = Y_1(z) \cdot H_1(z) + Y_2(z) \cdot H_2(z) \tag{3.17}$$

where $H_1(z)$ and $H_2(z)$ are the digital cancellation logics (DCLs) to cancel the quantization error of the first stage i.e. $E_1(z)$. $Y_1(z)$ and $Y_2(z)$ represent the outputs of the first and second stages, respectively. Assuming $H_1(z) = -z^{-1}$ and $H_2(z) = (1 - z^{-1})^2$, the quantization error of the first stage, $E_1(z)$, is ideally cancelled, while $E_2(z)$ is shaped by a fourth-order NTF.

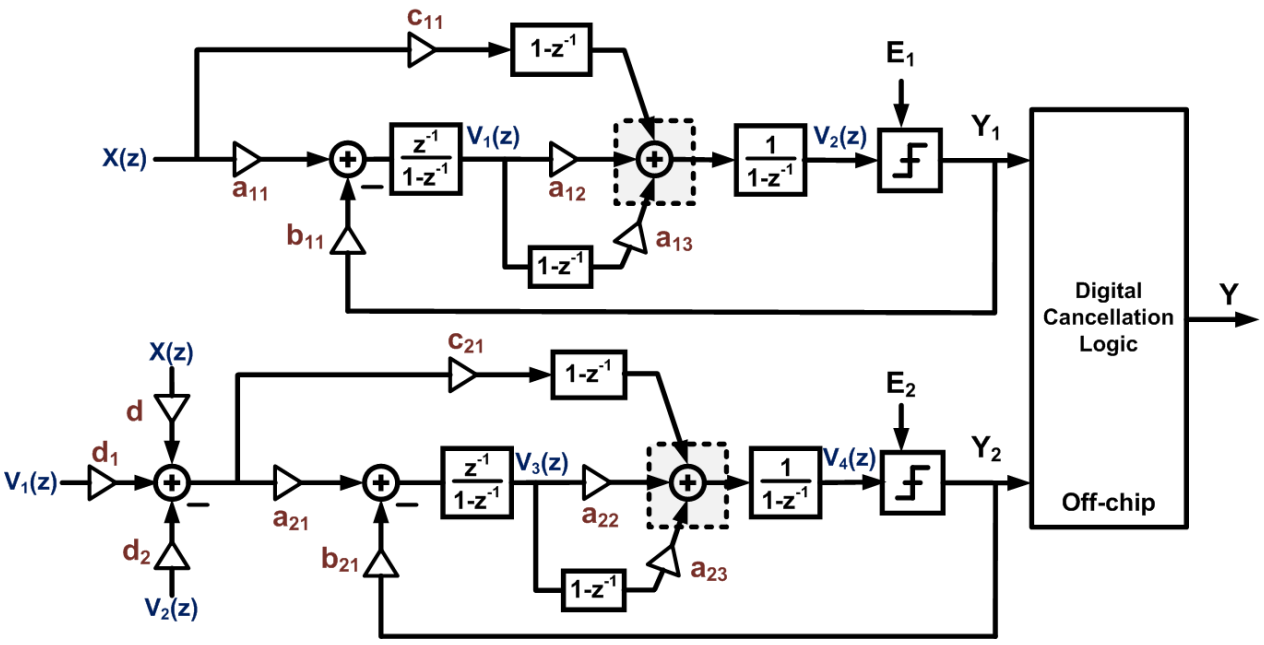


Figure 3.4 System-level diagram of the proposed adder-less MASH ΔΣM.

3.6 High-level Synthesis

The analysis presented above considers ideal ΔΣM building blocks. However, this ideal performance degrades in practice by the action of circuit error mechanisms [65]. A detailed analysis of the main nonidealities is therefore necessary in order to set the electrical specifications of the ΔΣM sub-circuits and to optimize their design.

3.6.1 Modulator Loop Filter Coefficients Scaling

The proposed adder-less MASH ΔΣM, depicted in Fig. 3.4, is synthesized with an NTF of $(1 - z^{-1})^4$, and all loop coefficients are initialized to one, while the output swing of each integrator is not considered. Therefore, it is more likely that the integrators will be saturated in an actual implementation if the output voltage level becomes critically large. Moreover, distortion, which deteriorates the performance of the ΔΣM, is the major consequence of the saturated integrators. Therefore, it is beneficial to observe the integrator output swings and to properly scale the coefficients of the modulator in order to guarantee a reasonable signal swing at each integrator output. This results in a reduced power consumption and an improved dynamic range (DR).

Behavioral simulations are carried out to monitor the output swing of all integrators versus input signal level, as shown in Fig. 3.5. Fig. 3.5(a) shows the output swing of all integrators

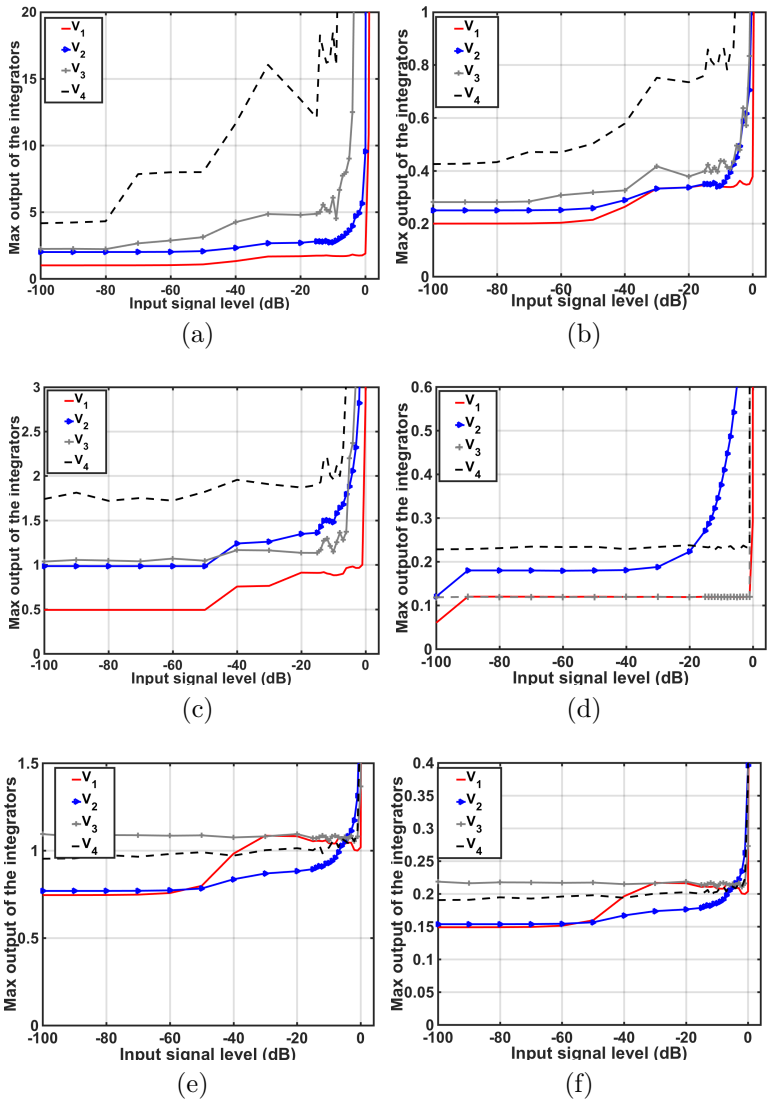


Figure 3.5 Integrator output swing (normalized to the ΔΣM full scale) versus input signal level : (a) Single-bit modulator synthesized through an NTF of $(1-z^{-1})^4$ and before scaling, (b) Single-bit modulator through an NTF of $(1-z^{-1})^4$ and after scaling, (c) 1.5-bit modulator synthesized through an NTF of $(1-z^{-1})^4$ and before scaling, (d) 4-bit modulator synthesized through an NTF of $(1-z^{-1})^4$ and before scaling, (e) Single-bit modulator synthesized through an NTF with an out-of-band gain of 1.5 ($H_{inf} = 1.5$) and before scaling, (f) Single-bit modulator synthesized through an NTF with an out-of-band gain of 1.5 ($H_{inf} = 1.5$) and after scaling.

while all coefficients are initialized to one resulting in an overall NTF of $(1-z^{-1})^4$. It is clear that the input of the first integrator must be scaled down by a factor of 8 to accommodate integrator's output swing in sub-1-V environment. This factor must be larger for the second and third integrators. It must be mentioned that larger scaling down factor leads to higher integrating capacitor value for a given sampling capacitor, and hence increased modulator

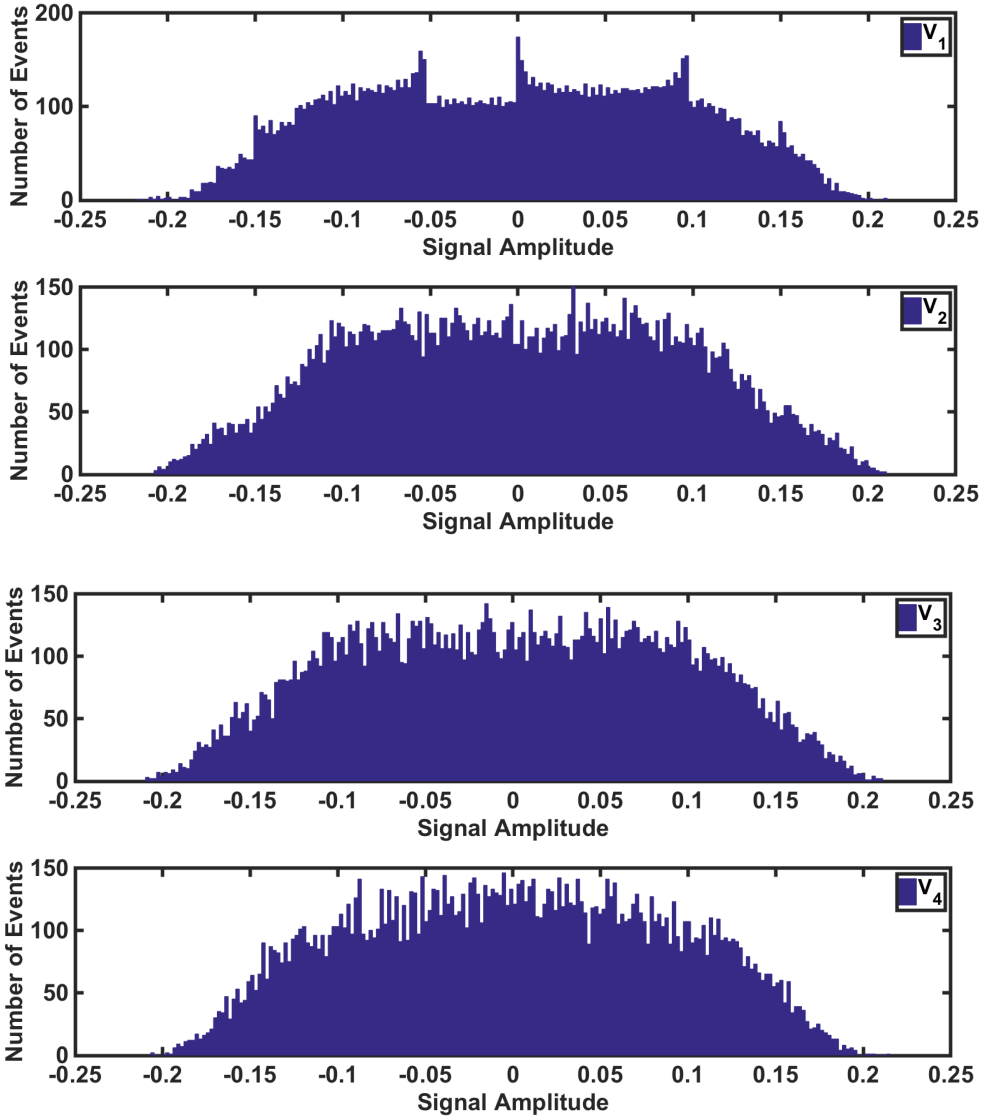


Figure 3.6 Histogram of the integrator output swings relative to the FS voltage.

power consumption. The fourth integrator is problematic as an unbounded output swing is observed at its output. In this condition the modulator tends to be unstable. Figure 3.5(b) shows the scaled modulator with a factor of 8. Note that, even using such a large scale factor for all integrators, an unbounded output swing is obtained at the output of the fourth integrator. As stated above, multi-bit quantization alleviates this issue at the expense of requiring DAC linearizion techniques, with a resulting penalty in power consumption. Fig. 3.5(c) and (d) shows the output swing of the integrators with a 1.5-bit and a 4-bit quantizer, respectively. For the case of a 1.5 bit quantizer per stage, the modulator still needs to be scaled down with large factors.

Table 3.1 Coefficients of the Proposed ΔΣM after Scaling

Coefficient	a_{11}	a_{12}	a_{13}	b_{11}	c_{11}	a_{21}
Value	0.15	0.3	0.75	0.15	0.15	0.15
Coefficient	a_{22}	a_{23}	b_{21}	c_{21}	d	$d_{1,2}$
Value	0.3	0.75	0.15	0.15	1	5

As a single-bit quantizer is assumed in this design, the NTF out-of-band gain (H_{inf}) is reduced to 1.5 and the coefficients of the modulator are re-synthesized. As shown in Fig. 3.5(e), the output swing of all integrators are bounded to 1 before scaling of the modulator. The output swing of integrators after coefficient scaling is shown in Fig. 3.5(f). It can be seen that the output swings do not tend to be saturated even close to an input level of 0 dBFS.

The output swing of the integrators are better illustrated in the histograms depicted in Fig. 3.6, where a −6-dBFS input signal level is considered after coefficients scaling. As can be seen from this figure, the output swings for all integrators are within 23% of the full-scale (FS) voltage. Due to such a relaxed headroom requirement, a high slew-rate OTA is not required, resulting in the ability to design a lower power circuit. The coefficients selected for the modulator after scaling are summarized in Table 3.1.

3.6.2 Sampling Capacitor of the Front-end Integrator

Careful selection of the sampling capacitor, especially for the first integrator, is an important task since it determines the $\frac{KT}{C}$ noise, which constitute the ultimate limiting factor in the noise floor of the modulator. On the other hand, the front-end sampling capacitor has a direct contribution on the capacitive load of the integrator and hence, on the settling requirement and the power consumption. The procedure given in [4] is followed to determine the sampling capacitor of the first integrator. In this design, for the target signal to noise ratio (SNR) of 90 dB at −3-dBFS, the signal power is $\overline{v_s^2} = 0.25$ V^2. Therefore, the in-band noise of $\overline{v^2}_{n,in-band} = 2.5 \times 10^{-10}$ V^2 results in total noise of $\overline{v^2}_n = 3.2 \times 10^{-8}$ V^2 for an OSR of 128. The calculated sampling capacitor would thus be of about 0.5-pF. Ensuring some design margin, the final sampling capacitor is selected to be 1-pF. It should be noted that the integration capacitor can be calculated according to $a_{11} = \frac{C_{s1}}{C_{i1}}$. A behavioral simulation is also carried out to optimize the integration capacitor of the first integrator, as shown in Fig. 3.7. The maximum in-band noise (IBN$_{max}$) is monitored as a function of the first integrating capacitor. Having the integrating capacitor of 6.7 pF results in an IBN$_{max}$ of about −105 dB. Considering that $a_{11} = 0.15$, the sampling capacitor is calculated as 1-pF,

which confirms our calculations.

3.6.3 OTA Specifications

The settling behavior of the integrator at the end of integration phase, which depends on the OTA parameters i.e. finite DC-gain, unity gain-bandwidth (GBW) and slew-rate (SR), play a crucial role in the overall performance of a high-resolution $\Delta\Sigma$M. This requires careful design of these parameters to ensure proper operation. However, overdesigning parameters in order to meet the requirements is not a viable approach as it would result in excessive power consumption, a critical parameter to minimize in the target low-power devices. Therefore, the objective of this section is to determine the minimum requirements for the OTAs used in the integrators of the proposed $\Delta\Sigma$M.

Since GBW and SR both determine the settling behavior of the modulator, it is beneficial to examine the simultaneous effect of GBW and SR, depicted in Fig. 3.8. It must be mentioned that the integrating capacitor of the first integrator is set to 6.7-pF for this simulation. As can be inferred from this simulation, to attain the target effective number of bit (ENOB) of 14-bit, the GBW and SR need to be more than 20-MHz and 15-V/μS, respectively. Giving some margin helps to avoid SNDR degradation due to other circuit imperfections not considered at this design stage.

Finite DC-gain of the OTA determines the accuracy of the final settled value at the end of the integration phase. An isolated evaluation is performed to extract the IBN_{max} of the modulator as a function of OTAs' DC-gain, as shown in Fig. 3.9. It should be mentioned that this evaluation is performed for the scaled modulator with a -6-dBFS sinusoidal input at the OSR of 128. As can be seen from this figure, the ideal quantization noise floor remains intact down to about 50-dB OTA DC-gain. This value could be scaled down for the rest of the integrators.

3.6.4 Jitter effect

It is well-known that a SC-$\Delta\Sigma$M is less sensitive to clock jitter error as compared to its CT counterpart and this is due to the fact that the SC-integrator is designed to be well-settled within half of the clock period. The jitter modulated by the signal frequency, however, might degrade the performance of the SC-$\Delta\Sigma$M when increasing the input frequency. Assuming that the clock jitter has a Gaussian random distribution with the standard deviation of $\sigma_{\Delta t}$, the signal to jitter noise ratio (SJNR) is expressed as follows [4] :

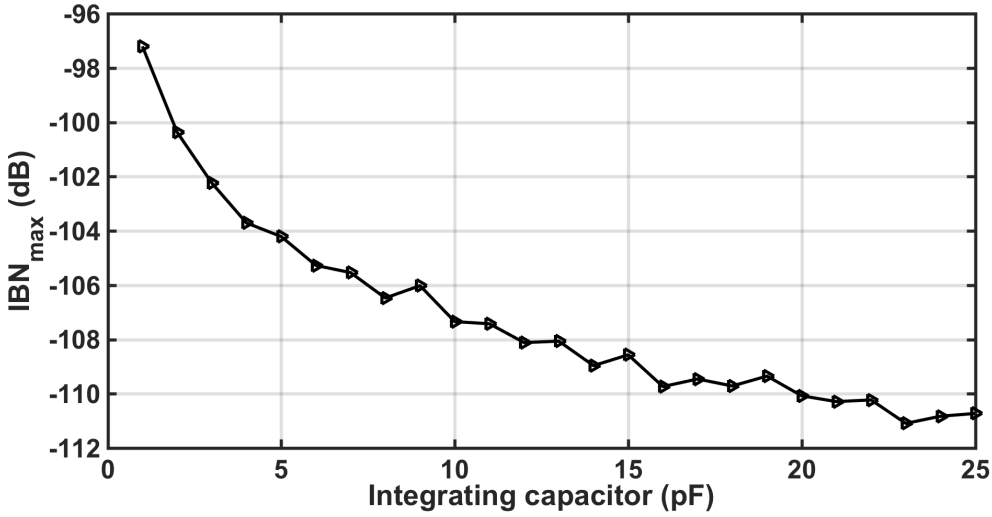


Figure 3.7 Maximum IBN versus integration capacitor size of the first integrator.

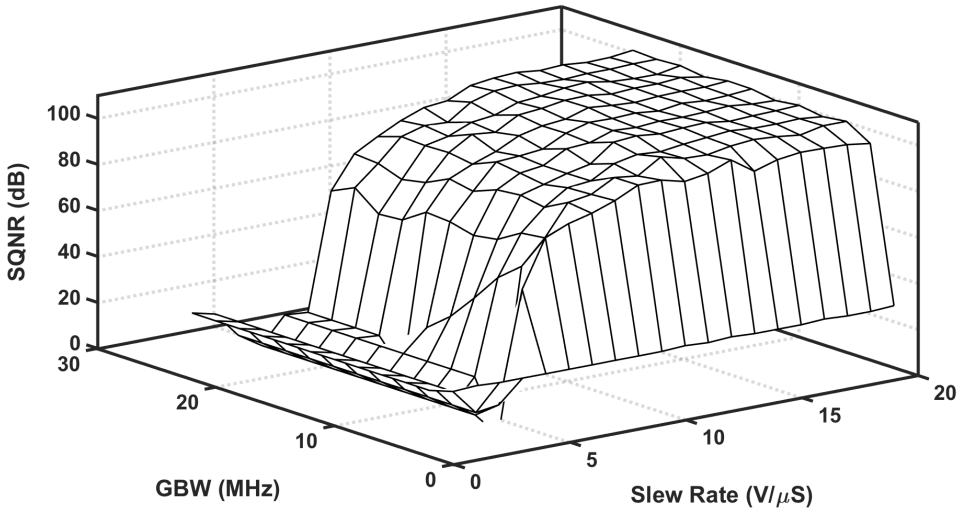


Figure 3.8 SQNR versus GBW and SR in the front-end OTA.

$$SJNR = \frac{OSR}{4\pi^2 f_{in}^2 \sigma_{\Delta t}^2} \tag{3.18}$$

where f_{in} is the input signal frequency. To examine the effect of clock jitter while increasing the input signal frequency, a behavioral simulation is carried out as depicted in Fig. 3.10. It is shown that the proposed modulator can tolerate clock jitter of up to 400-ps without significantly SJNR degradation.

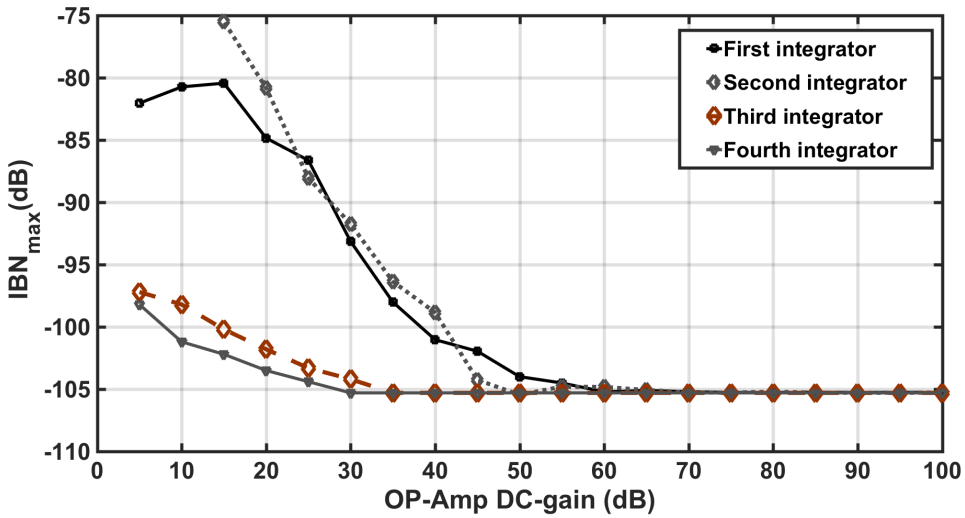


Figure 3.9 Maximum in-band noise versus OTA DC-gain.

3.6.5 Capacitor Mismatch

The integrator gain coefficients, depicted in Fig. 3.4, are implemented as capacitor ratios of $\frac{C_{s,i}}{C_{I,i}}$ $i = 1, ..., 4$. Therefore, any deviation of these values from the nominal ones, due to variation in process technology parameters or changes the pole/zero location of the NTF may make the modulator unstable. In the case of single-loop ΔΣMs, a small deviation is not significant since the filtering provided by the integrators remains unchanged. Moreover, capacitor mismatch may have a significant impact on the performance of the MASH ΔΣM since the gain deviation of the integrators is not compensated by the digital coefficients of the DCL, and consequently the modulator has a quantization error leakage at its output with low order noise shaping.

Considering the OTAs' specifications determined in the previous section, the capacitor mismatch requirement is determined by executing a 500-run Monte Carlo analysis with a Gaussian distributed random mismatch. As depicted in Fig. 3.11, SNDR deviates 2-dB from its nominal value for 0.1% coefficient mismatch. Capacitor mismatch beyond 0.1% is a pessimistic design scenario, as a capacitor mismatch lower than 0.1% can be achieved by careful layout techniques.

Table 3.2 summarizes the results of the high-level sizing process, considering the main circuit non-ideal parameters associated to the ΔΣM building blocks. These parameters define the electrical specifications for the circuit-level design described in the next section.

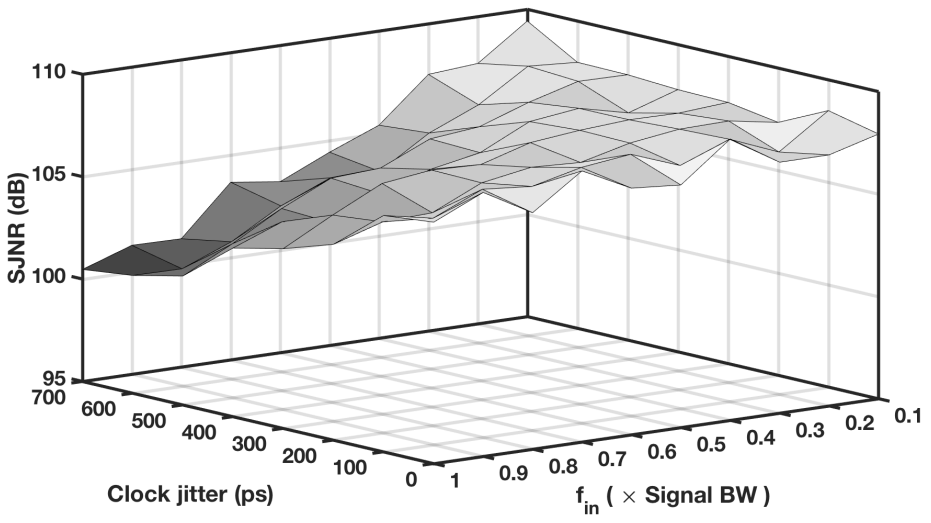


Figure 3.10 SJNR versus input signal frequency and clock jitter standard deviation.

3.7 Circuit-Level Implementation

Figure 3.12 depicts a conceptual schematic of the proposed adder-less MASH 2-2 $\Delta\Sigma$M along with the its clock-phase timing diagram. Although a single-ended schematic is shown for simplicity, the actual implementation is fully differential. To realize both stages of the proposed modulator, a delayed integrator followed by a non-delayed integrator serve as a loop-filter as well as summing amplifier. The first integrator samples the input signal at Φ_1 and the integration is performed at subsequent Φ_2. Meanwhile, the output of the first integrator is directly sampled by the second integrator at Φ_2 and integrated during the Φ_1 phase. The second integrator also sums the two other signals coming from the input signal and output of the first integrator, simultaneously. Proper switching techniques are employed to guarantee low switch on-resistance and hence offering enough settling accuracy during the operation time. Locally bootstrapped switches (BT-SW) [15], highlighted in Fig. 3.12, are utilized in the signal paths to provide enough sampling linearity to avoid degrading the performance of the proposed modulator over a wide range of input swings. As explained earlier, the integrating capacitor of the first integrator needs to be 6.7-pF to achieve a half SNDR of about 95 dB. For the rest of the integrators, the integrating capacitors are scaled-down to 1-pF, due to the noise suppression inside the loop, and to diminish the power consumption. The rest of capacitors are determined according to the corresponding coefficients.

Non-overlapping clock phases, i.e. Φ_1 and Φ_2, are needed for normal operation of the SC-$\Delta\Sigma$M. The delayed version of the main phases i.e. (Φ_{1d} and Φ_{2d}) are also needed to diminish the clock feed-through. Analog implementation of the switches can be problematic when the supply voltage is reduced to half of the nominal voltage rating of the 0.18-μm CMOS process

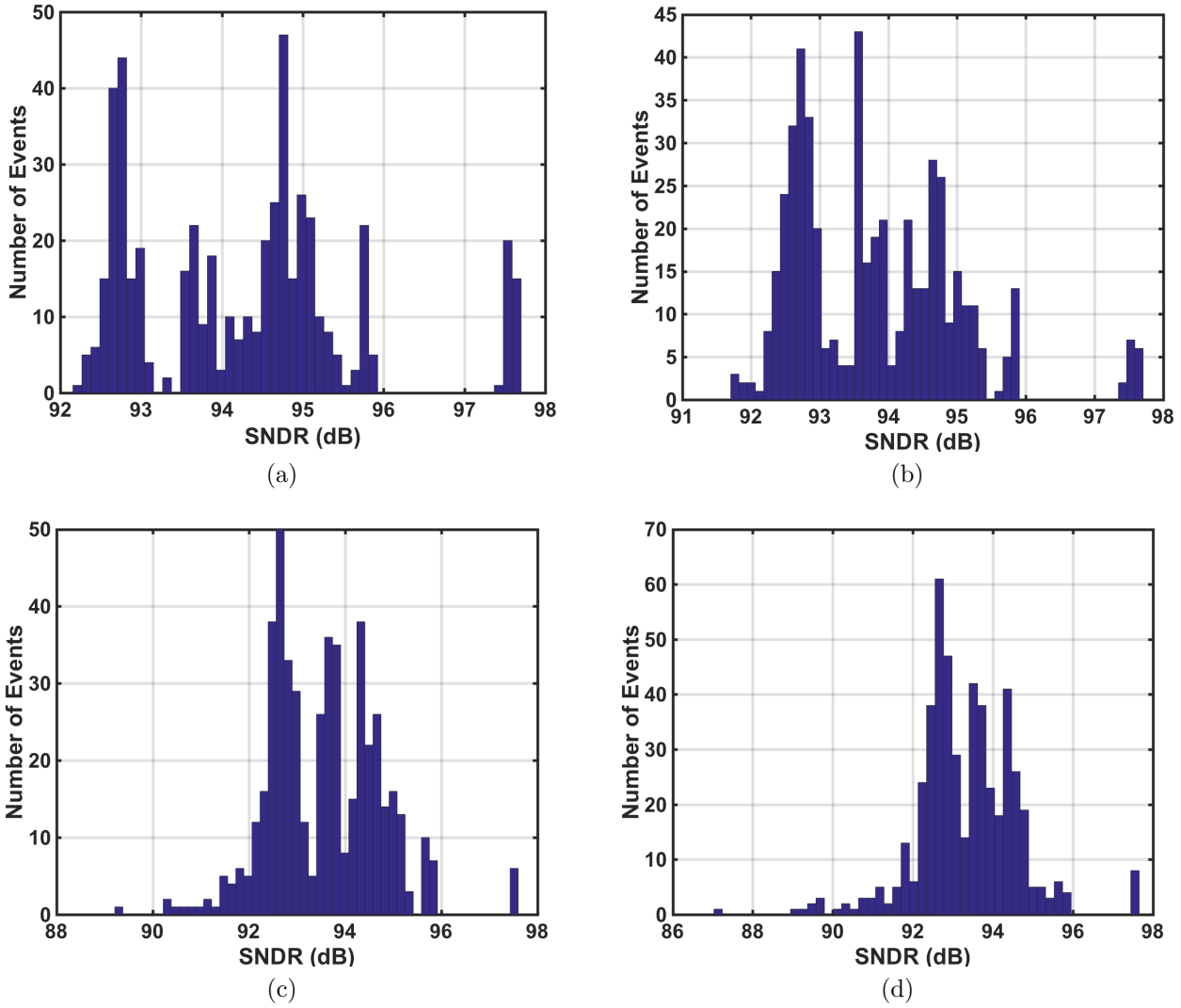


Figure 3.11 Monte Carlo simulation results by considering a capacitor-ratio mismatch of : (a) 0.1%, (b) 0.2%, (c) 0.3% and (4) 0.4%.

(i.e. 1.8-V). To circumvent this issue, locally BT-SW [15] are used in the ΔΣM chip. Dummy switches are also utilized for the sake of clock feed-through suppression.

3.7.1 Proposed Self and bulk Biased OTA

The selection of an appropriate OTA topology is the most critical part of the design of a ΔΣM especially in the case of low-power high-resolution ΔΣMs. Compared to other OTA topologies, inverter-based OTAs have been employed in different ΔΣMs [66]-[67]. One of the main drawbacks of these kinds of OTAs is that they need a dedicated low dropout regulator to make some of their performance parameters insensitive to process, voltage and temperature

Table 3.2 High-Level Sizing of the Proposed ΔΣM

Simulation setup @ −6-dBFS, $OSR = 128$				$SNDR$ (dB)
Quantization noise only				108
Integrating capacitor of 6.7-pF for the first integrator				95.7
OTAs	DC-gain (dB)	OTA1	50	93.6
		OTA2,3,4	40	
	GBW (MHz)	OTA1	> 20	94.85
		OTA2,3,4	> 10	
	SR (V/μs)	OTA1	> 15	
		OTA2,3,4	> 5	
Quantizer	Hysteresis + offset (mV)	Q1	70	95.24
		Q2	70	

(PVT) [68]-[69]. To tolerate PVT variations, a dynamic biasing technique has also been addressed in [70] at the expense of limiting the bandwidth of inverter-based OTA which makes this technique undesirable for MHz range sampling frequency. To accommodate the speed limitation of the dynamic biasing technique, an active parasitic compensation is proposed in [71] at the expense of extra current drawing due to the use of copying the quiescent current of the inverter and adding more circuit complexities. It is known that self-biasing techniques provide robustness against PVT variation and remove the need for regulators. Thus, a self-biased single-ended inverter-based OTA was introduced in [72], while [73] addresses a pseudo-differential inverter-based OTA with complex circuities and both are biased in the strong inversion. It is favorable to bias the inverter-based OTA in the weak inversion to maximize $\frac{g_m}{I_D}$ and minimize the power consumption [71]. However, it was shown that sub-threshold circuits do not meet the requirements over slow and fast process corner [60].

As shown in Section 3.6, unlike [67] where an OTA with a gain boosting technique is required, a DC-gain of 50 dB is sufficient to maintain the SNDR of the proposed ΔΣM intact. Therefore, the main objective is to keep the structure of the inverter-based OTA as simple as possible while making it robust over process corner. Beginning with the proposed self-biased (SB) inverter-based OTA in the weak inversion region, it will be shown that it provides the target DC-gain over the process corners. However, it fails at slow process corner or low V_{DD}. The aforementioned issues are avoided by proposing a SBB inverter-based OTA as described in the following sections.

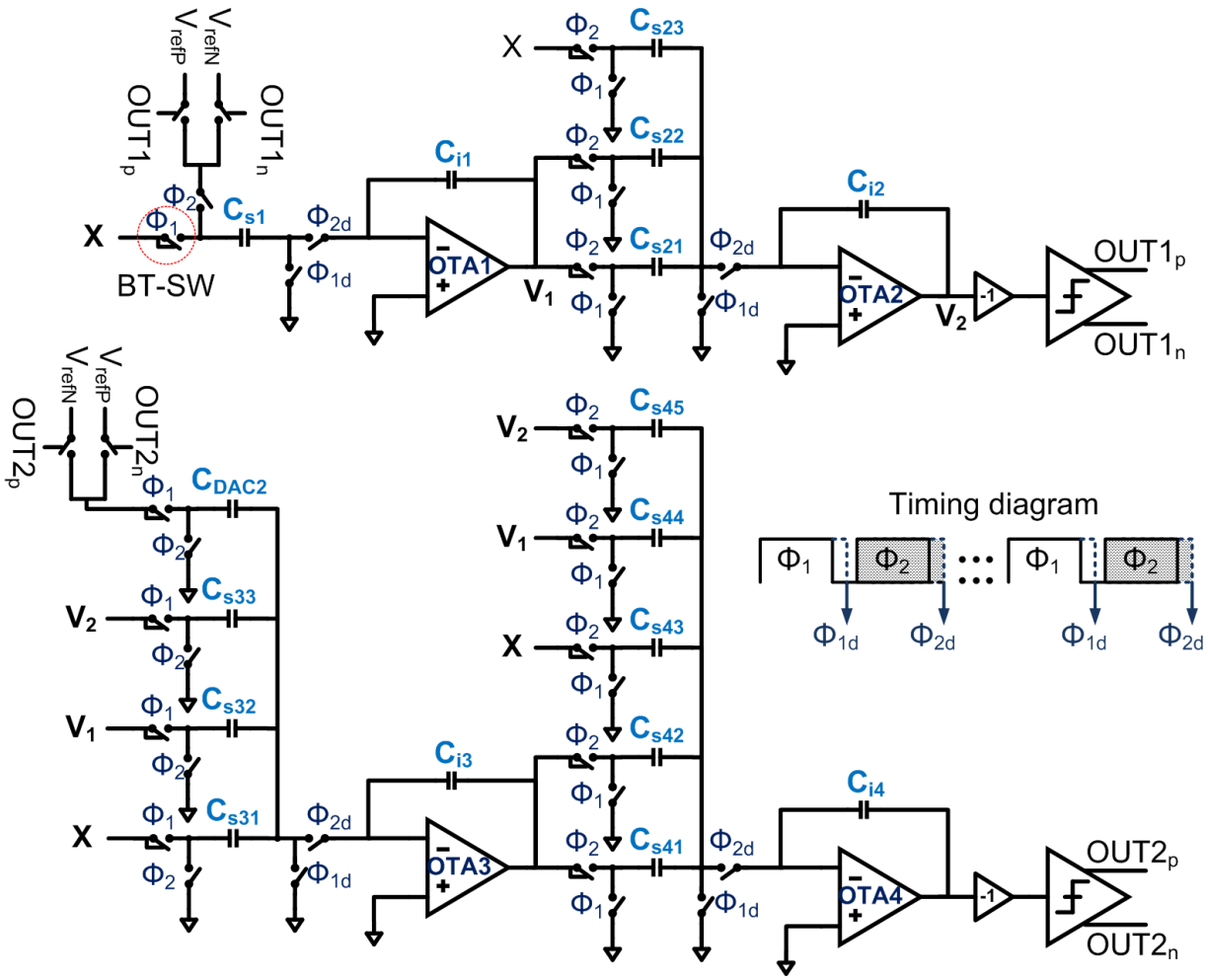


Figure 3.12 Schematic (single-ended) of the proposed adder-less MASH 2-2 ΔΣM.

Power-Efficiency Considerations

Figure 3.13(a) shows the schematic of a SB fully differential current starved inverter-based OTA biased in the weak inversion. Due to the use of a differential OTA, a common mode feedback (CMFB) circuit is used to sense the output common-mode voltage and maintain the output voltage at a certain level which is the mid-supply voltage, i.e. 0.45-V. Transistors $M_{5,6}$ along with the CMFB make the DC-gain of the SB inverter-based OTA robust to PVT variation by providing a negative feedback loop. It will be shown that the DC-gain of the OTA is always above 51-dB over the process corners which meets the target specifications. A SC implementation of the CMFB, shown in Fig. 3.13(c), is used to save on power consumption and not to limit the swing of the OTAs. The switches connected to the OTA outputs are implemented as locally BT-SW to accommodate wider voltage swings.

The OTA structure in Fig. 3.13(a) presents a very high transconductance efficiency whereas

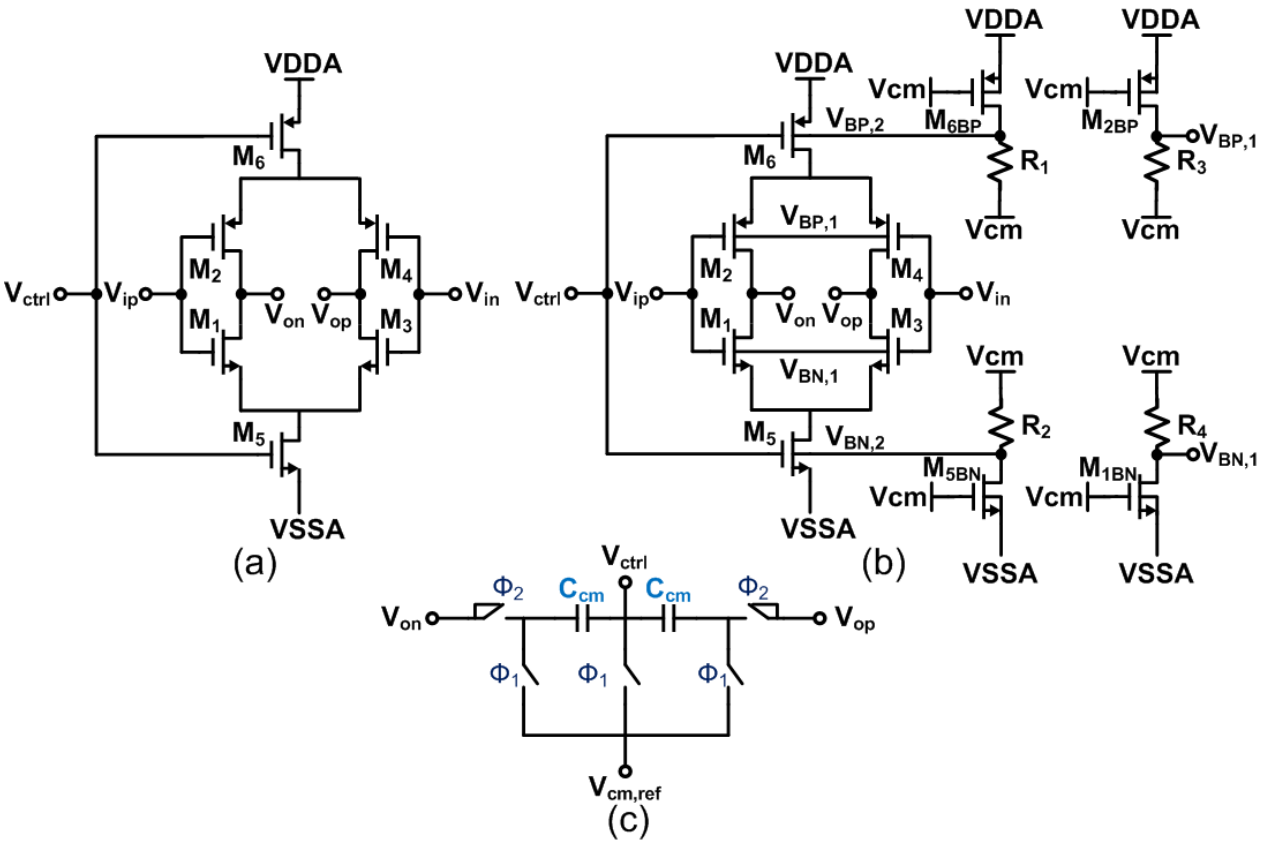


Figure 3.13 Inverter-based OTA, (a) Proposed SB inverter-based OTA in the weak inversion, (b) Proposed SBB inverter-based OTA in the weak inversion, (c) CMFB circuit.

both devices (i.e. NMOS and PMOS) contribute to the overall transconductance of the OTA so that $G_{m,total} = g_{m,NMOS} + g_{m,PMOS}$. Assuming the same transconductance for both NMOS and PMOS, the tail current of the inverter-based OTA can be expressed as follow :

$$I_{tail} = GBW.2\pi.n.V_T.C_L \tag{3.19}$$

Comparing (12) to the results shown in [59], not only does the inverter-based OTA exhibit a lowest tail current, but it also shows a rail-to-rail output swing, resulting in a higher SR. Unlike floating inverter-based OTAs, the proposed SB OTA in Fig. 3.13(a), is *sandwiched* between a PMOS current source at the top and an NMOS current sink at the bottom. These current source/sinks help to improve the positive power supply rejection ratio (PSRR) and negative PSRR as well, of course at the expense of extra voltage headroom. This is not an issue since all of the transistors are biased in the weak inversion region. Furthermore, MOS operation in weak inversion can provide a large value of $\frac{g_m}{I_D}$ in comparison to transistors operating in strong inversion, resulting in a better current efficiency [74].

Noise

In addition to the thermal noise, dictated by the sampling capacitor, the input referred noise of the OTA is another limiting factor that needs to be taken into account. In this design, $L_{1-4} = L_n$, $W_{2,4} = 3\times W_{1,3} = 3\times W_n$ and μ_n=$3\times\mu_p$ are chosen, resulting in total input referred noise given by :

$$\overline{v_{n,in}^2} = \frac{4}{3}\cdot\frac{K_F}{C_{ox}W_nL_n}\cdot\frac{1}{f} + \frac{4kT\gamma}{g_m} \tag{3.20}$$

where K_F is the flicker noise coefficient ; f is frequency ; C_{ox} is the oxide capacitance, g_m, W and L represent the transconductance, width and length of the transistor, respectively ; k is the Boltzmann's constant ; T is the absolute temperature value and γ is approximately $\frac{1}{2}$ in the weak inversion region.

Flicker noise is the dominant noise source at low frequencies. In order to attenuate its effect, well-known chopper stabilization and correlated double sampling techniques can be used. However, the first one may modulate the shaped high-frequency quantization noise back down to the baseband and the latter can cause additional thermal noise and coupling clock noise induced by the added switches in the sampling front-end [75]. Considering the above issues, none of the mentioned flicker-noise attenuation techniques are used in this design. Instead, device sizes of the input transistors are increased to suppress flicker noise [16].

PVT Consideration

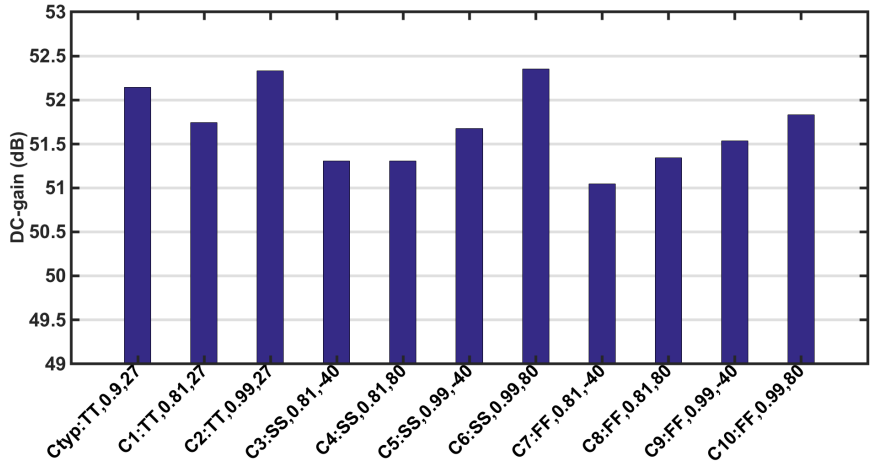
As mentioned earlier, MOS transistors are biased in the weak inversion in the proposed OTA and in such a region MOS parameters show a great fluctuation in the presence of PVT variations resulting in a sever degradation in the performance of the proposed ΔΣM. Taking PMOS transistors into account, i.e. $M_{2,4,6}$ for example, this fluctuation can be described as follows. In the presence of the slow-slow (SS) corner, the transconductance and drain current of PMOS transistors decreases resulting in a malfunction in the proposed ΔΣM. This fluctuation shows itself an increase in the power consumption when process corner is fast-fast (FF). To mitigate this issue, bulk biasing technique is employed to modify the proposed OTA as depicted in Fig. 3.13(b). As shown in this figure, sensing transistors, which are biased in the weak inversion, sense the fluctuation of the main transistors and decide proper reaction. In the presence of the SS corner, the sensing transistors, M_{2BP} and M_{6BP} for example, detect the fluctuation and thus reducing the drain current. Therefore, V_{BP1} and V_{BP2} are decreased and thus the threshold voltage, $V_{th,p}$, of the PMOS transistor resulting in an increase in the transconductance and drain current of the PMOS transistors. When at FF

process, the drain current of the sensing transistor increases resulting in an increase in V_{BP1} and V_{BP2} and so does the $V_{th,p}$. However, an additional positive and negative levels must be introduced to let this technique be effective at the FF process [76]. As will be shown, the SB inverter-based OTA fails at SS process or low V_{DD} and meets the requirements at the FF process. Therefor, no additional positive and negative levels are introduced in the proposed SBB inverter-based OTA.

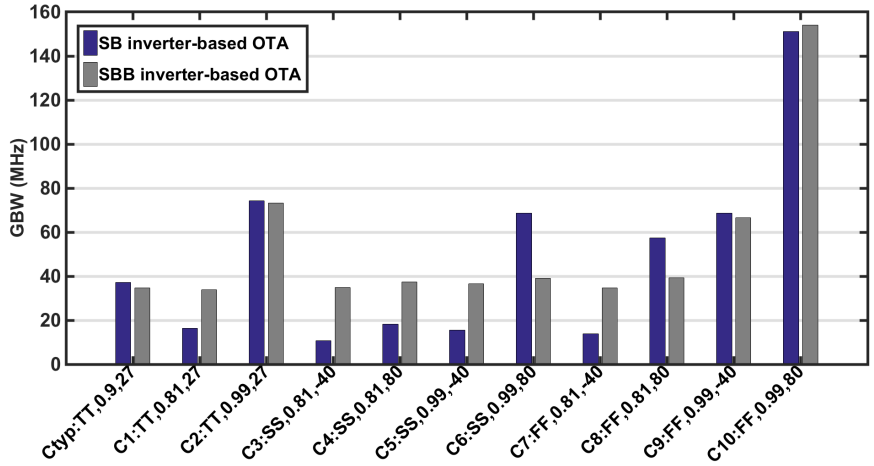
All integrators in Fig. 3.12 have been designed using SBB inverter-based OTAs depicted in Fig. 3.13(b). However, due to the different electrical specifications required for each OTA (see Table 3.2), two different OTA designs are used for the first integrator (OTA1) and the rest of the integrators (OTA2,3,4), respectively. Except for the first OTA, the other OTAs are relatively less critical and the current and performance are hence scaled down.

Figure 3.14 shows the simulation results of some AC performance metrics and power consumption of the OTA1, considering different corners and typical condition. These simulations include 10% variation in the 0.9-V supply voltage over three temperature values, namely : $-40°$C, 27°C and 80°C. Corner cases are defined in the figure (i.e, condition, supply, temperature). As shown in Fig. 3.14(a), a worst-case DC-gain of 51.04 dB (about 1-dB less than the typical condition) is observed in this analysis. Such a DC-gain meets the requirement indicated in Fig. 3.9 and table 3.2. Figure 3.14(b) illustrates the GBW of the proposed OTA with/without bulk biasing technique. For the typical corner, the proposed OTA shows a GBW of 37.18 MHz and 34.61 MHz with and without bulk biasing technique. At the SS process corner, C3 corner for example, the GBW levels off to 10.67 MHz when bulk biasing is not activated while the GBW is restored to a value of 34.8 MHz with activated bulk biasing. Similarly, the same compensation can be performed when low V_{DD} occurs. Figure 3.14(c) shows the power consumption of the proposed SBB inverter-based OTA across different corners. Again C3 corner for an example, due to an increase in the drain current of PMOS transistor, power consumption levels up to 56.2-μW (96% of the typical value). The phase margin of the SBB inverter-based OTA is 86.34° with deviation range of less than 2% across different process corners.

As mentioned earlier, the proposed SBB inverter-based OTA can meet the GBW requirement over PVT variations. It is also worth examining the settling behavior of the proposed OTA. According to Spectre® simulation, depicted in Fig. 3.15(a), the SB inverter-based OTA's set-up time is 39.2-ns at the typical corner while it cannot completely settle-down at slow process corner, achieving 71-ns settling-time. SBB inverter-based OTA, however, properly settle-down within about 39.8-ns i.e. 20.3% of the sampling period. Figure 3.15(b) shows the simulated results of the proposed OTA over PVT variations. As can be seen from this figure,



(a)



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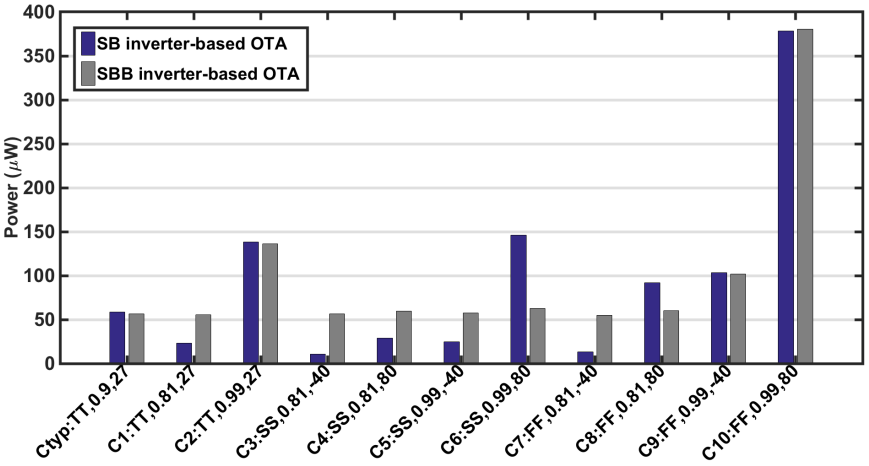


(c)

Figure 3.14 Simulated performance of the front-end SBB inverter-based OTA over PVT variations : (a) DC-gain, (b) GBW and (c) static power.

the failure over the slow process corner or low supply voltage can be restored by the proposed OTA such that the integrator can settle-down within less than 22% of the sampling period.

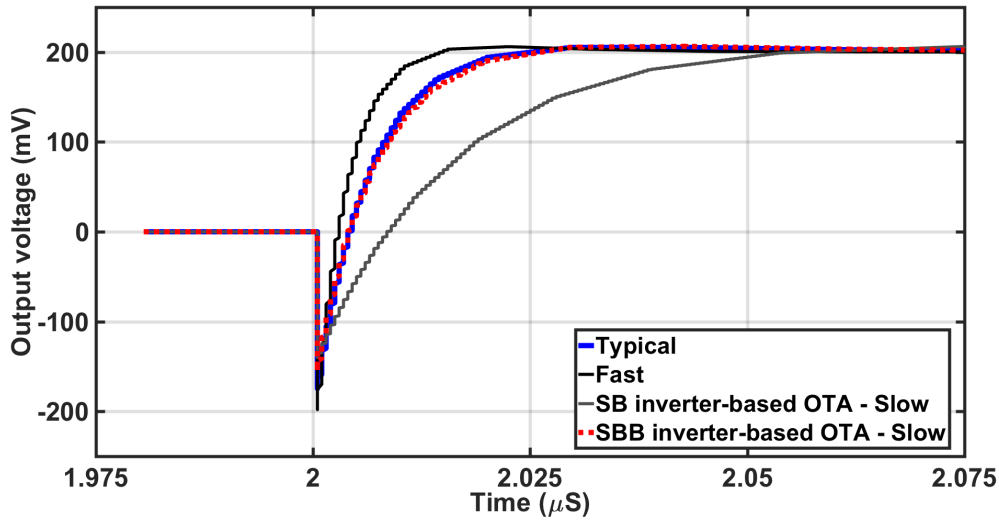
Table 3.3 lists the post-layout simulation results of the designed OTAs. Under typical-corner conditions, OTA1 has a DC-gain of about 52 dB and a GBW of 37 MHz, which is sufficient for the required modulator performance, as confirmed by behavioral simulations, according to Table 3.2. The other OTAs show a DC-gain of about 52 dB as well and a GBW of about 16 MHz. Although, 40-dB DC-gain is good enough to avoid SNDR degradation, the DC-gain is kept at 52-dB with a negligible power penalty.

PSRR Considerations

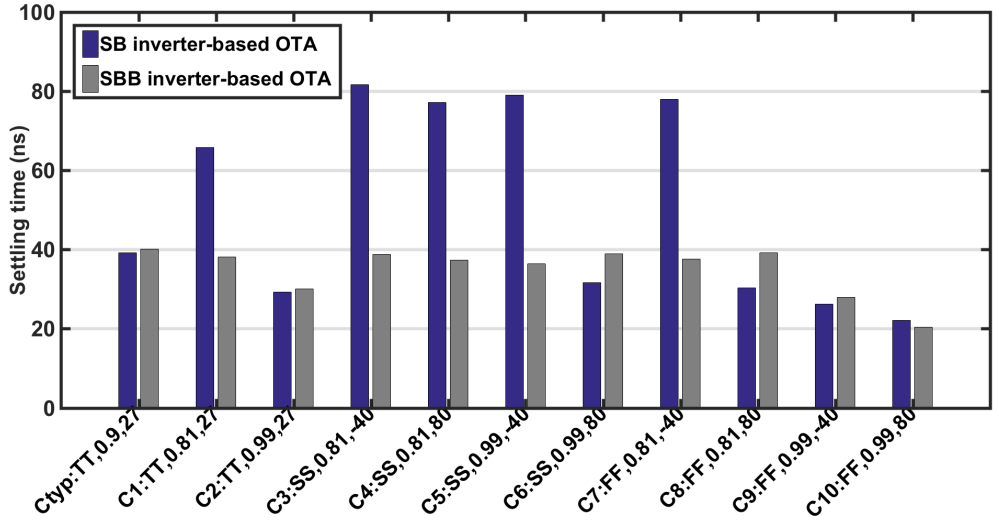
It is known that a single-ended inverter-based OTA shows a poor PSRR due to high supply voltage gain [67]. A pseudo-differential topology, as depicted in Fig. 3.13(b), is employed to improve the PSRR. Ideally matched input transistors results in an infinitely high PSRR. However, there is always mismatches between input transistors in the actual implementation. Fig. 3.16 illustrates the PSRR of the first OTA versus frequency for different transistor mismatch conditions. The OTA shows a positive PSRR of 76.5 dB and a negative PSRR of 83.4 dB for a 2% mismatch of only the NMOS input transistors i.e. $M_{1,3}$. For a 2% mismatch of only the PMOS input transistors, the OTA shows a positive and negative PSRR of 91.7 dB and 90.5 dB, respectively. Considering a 2% mismatch of both NMOS and PMOS input transistors, it is shown that the overall positive and negative PSRR are almost determined by the mismatch between the NMOS input transistors. The reason is that the aspect ratio of the PMOS transistor is three times that of the NMOS input transistors in the designed OTA. Therefore, special care must be taken when laying out the NMOS input transistors, $M_{1,3}$.

CMRR Considerations

Single-ended inverter-based OTA shows a common mode rejection ratio (CMRR) of 0 dB while pseudo differential inverter-based OTA suffers from a poor CMRR due to the lack of a tail current to regulate the total current flows through the inverter. However, the tail transistors, i.e. $M_{5,6}$, allow to improve the CMRR in the proposed SBB inverter-based OTA. The proposed OTA CMRR versus frequency is depicted in Fig. 3.17. The proposed OTA shows a CMRR of about 95 dB for 5% transistor mismatch over the desired 20-kHz signal bandwidth.



(a)



(b)

Figure 3.15 Simulated step response of the first integrator (a) comparison of SB and SBB inverter-based OTA for slow corner and (b) settling-time over PVT variations.

Table 3.3 Simulated Performance of the OTAs

Parameter	OTA 1	OTA 2,3,4
DC gain (dB)	52.15	52.07
GBW (MHz)	37.18	16.68
Phase margin (degree)	86.34	88.1
Supply voltage (V)	0.9	0.9
Power consumption (μW)	58.3	5.19

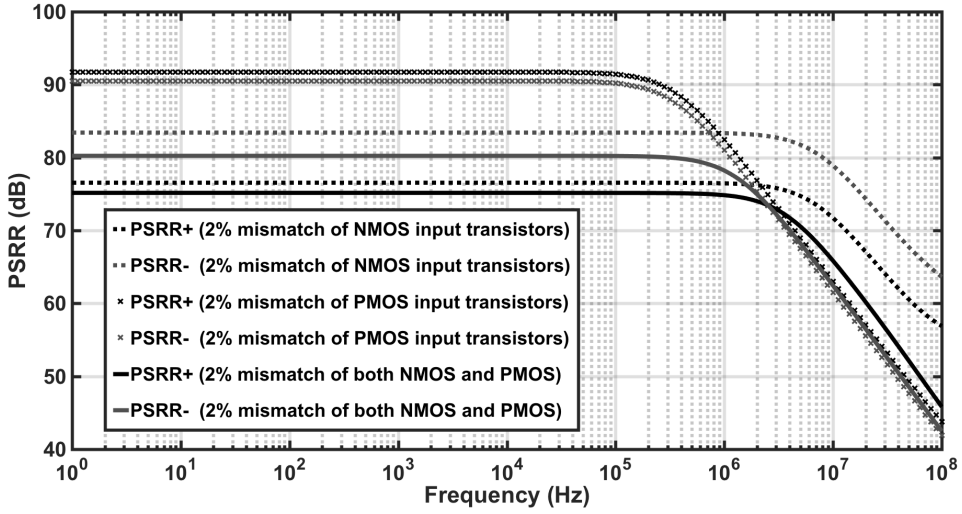


Figure 3.16 PSRR versus frequency.

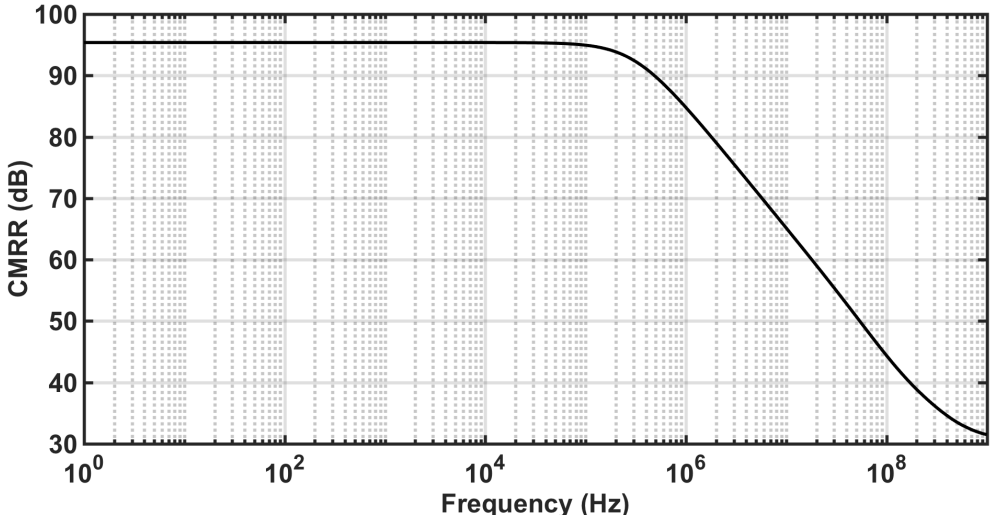


Figure 3.17 CMRR versus frequency.

3.7.2 Comparator

As stated earlier, a single-bit quantizer (i.e. a comparator) is used in the proposed modulator. A regenerative latch preceded by a SC-network and followed by an SR-latch, as depicted in Fig. 3.18, is used to implement the comparator in order to preclude the need for a power hungry pre-amplifier. The input capacitor, C_{in}, and the reference capacitor, C_{ref}, are pre-charged during Φ_1 while the SR-latch holds the output of the regenerative latch at the same clock phase. The comparator threshold voltage can be tuned by the ratio of the capacitors i.e. $\frac{C_{ref}}{C_{in}}$.

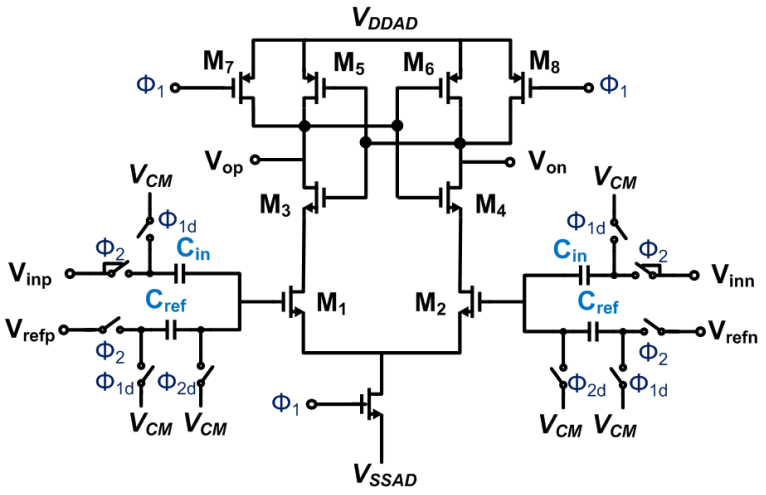
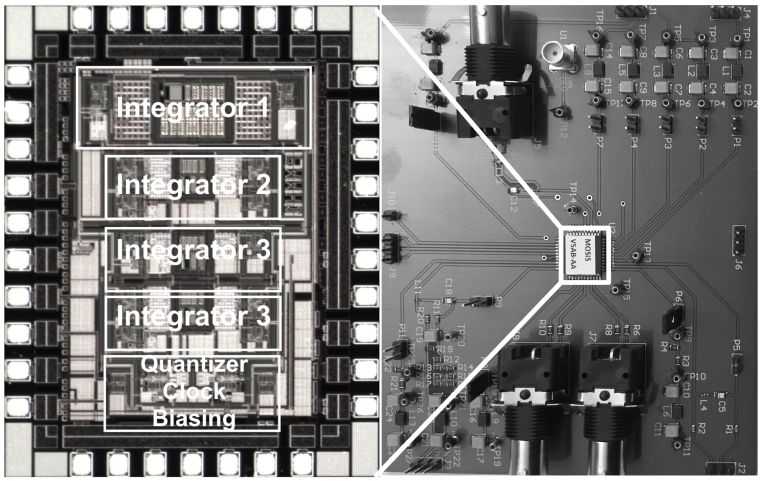


Figure 3.18 Latch-based comparator used to implement the 1-bit quantizer.

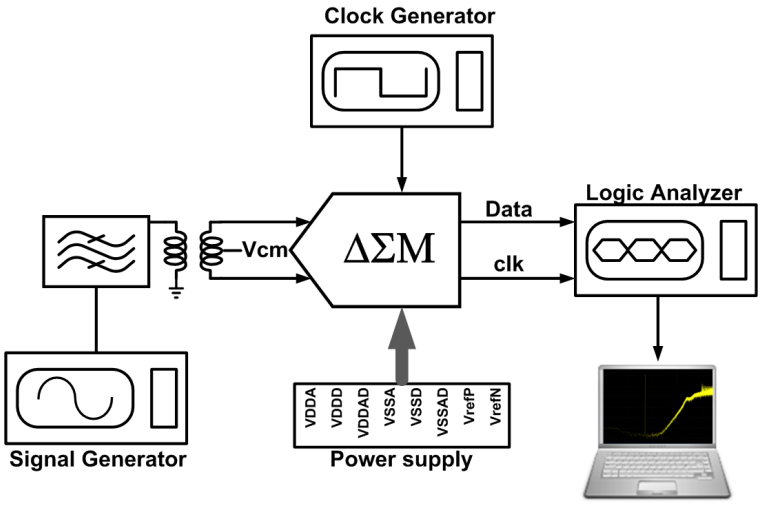
3.8 Experimental results

The proposed ΔΣM has been fabricated in a 0.18-μm 1P6M CMOS technology. Standard CMOS devices along with metal-insulator-metal (MIM) capacitors have been employed in the design. Arrays of capacitors are laid out in common-centroid fashion to provide matching and make the design immune across chip gradients. The layouts of the building blocks are designed fully symmetrical, when applicable, to match their differential signal paths. Analog, mixed signal and digital supply voltages are used to alleviate switching noise coupling. Reference voltage pins with decoupling capacitors are also used to suppress noise interference. The chip occupies an active area of 1.5 mm × 1.2 mm including pads. Fig. 3.19 shows the chip micrograph, test board and measurement setup. A fully differential input sinewave is applied using an audio precision signal generator. A single-ended input sinewave is band-pass filtered with a passive band-pass filter to suppress the harmonics of the signal generator and then converted to a differential signal using a balun. The digital outputs are stored in the memory of a logic analyzer and then transferred to a PC for subsequent processing in MATLAB.

A 5.2-kHz sinewave input signal with an amplitude of −6-dBFS is fed into the test board while the clock frequency is set to 5.12-MHz. The output spectrum of the modulator, acquired by average of 16 65536-point FFTs with Hanning window, is depicted in Fig. 3.20. Figure 3.21 shows the SNR and SNDR versus the input signal level in the audio band of 20 kHz. The modulator achieves an 86.4-dB peak SNDR, 88.7-dB peak SNR and 91-dB DR from a 0.9-V supply. The measured HD2 and HD3 are −109-dBc and −103-dBc, respectively. Although the input transistors of the first OTA have been sized large enough to suppress flicker noise and offset, a residue offset voltage is still observed. That is likely due to asymmetric charge



(a)



(b)

Figure 3.19 (a) Chip micrograph and test board and (b) Measurement setup.

injection and clock feed-through, and offset of the second integrator or quantizer. However, it is not a limiting factor in audio bands. The proposed ΔΣM consumes 103.4-μW from a 0.9-V supply. Figure 3.22 shows the breakdown of the power consumption between the different ΔΣM modules. As expected, the first integrator consumes 58% of the power, while the rest of integrators together consume 15% of the total power. Note that the capacitors of the second stage could be halved and the power consumption and GBW of OTA3 and OTA4 could potentially be scaled down further to reduce the overall power consumption. Due to the use of buffers for the clock generator as well as locally BT-SW, the digital blocks consume 27% of the total power.

Finally, Table 3.4 summarizes the measured performance of the proposed ΔΣM and compares its main metrics with the state of the art reporting on ΔΣMs intended for similar

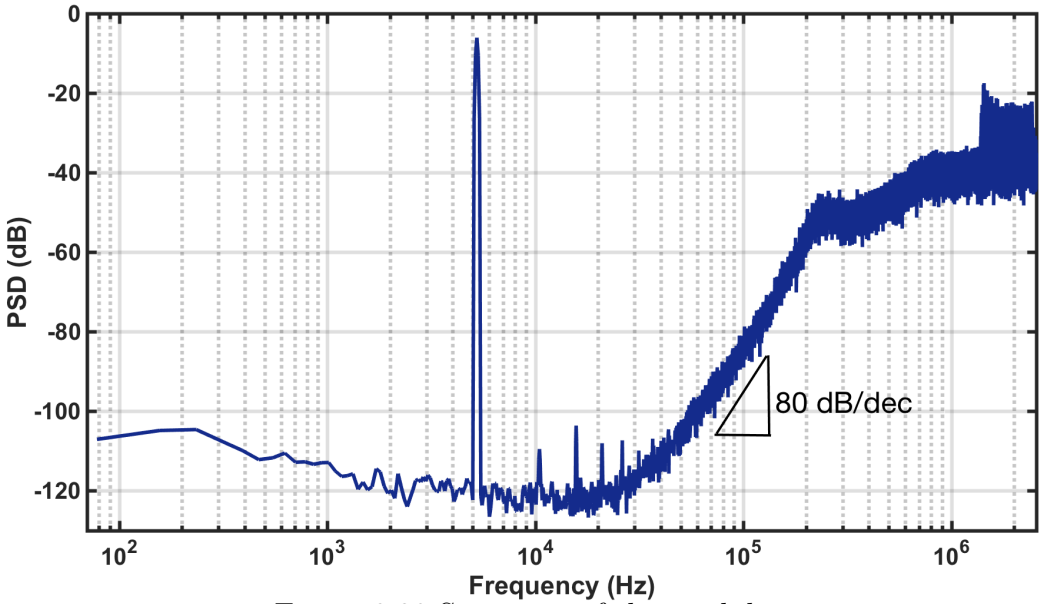


Figure 3.20 Spectrum of the modulator.

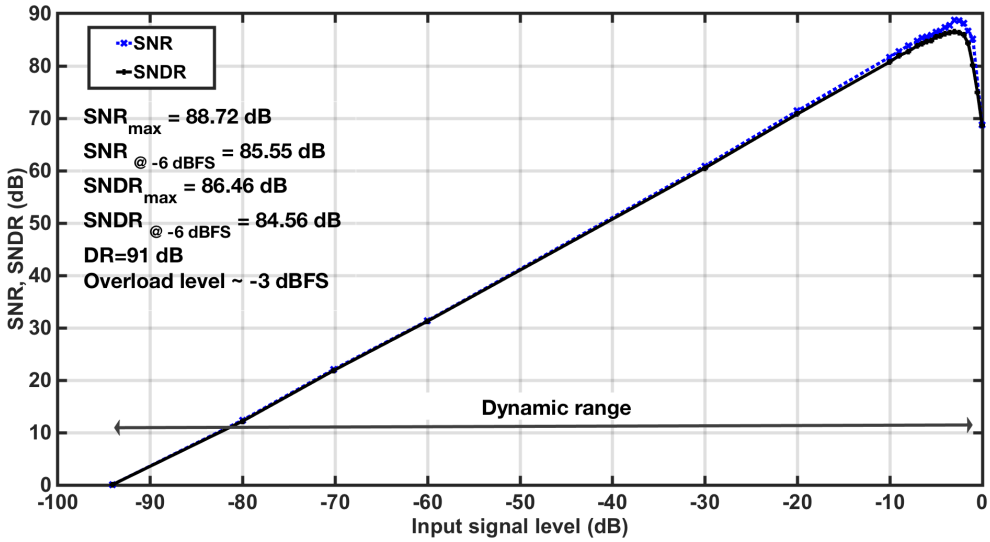


Figure 3.21 SNR, SNDR versus input signal level.

resolution-bandwidth specifications. Both the Walden and Schreier's figure-of-merits (FOMs) with SNDR and DR – given in (14) and (15)– are also included in the table for comparison purposes. Note that this work presents one of the best performance metrics compared to the state of the art, featuring 173.8-dB FOM_{DR} and 0.15-$\frac{pJ}{conversion}$ FOM_{SNDR}.

$$FOM_{SNDR} = \frac{Power}{2 \cdot BW \cdot 2^{2 \cdot \frac{SNDR-1.76}{6.02}}} \tag{3.21}$$

$$FOM_{DR} = DR + 10\log(\frac{BW}{Power}) \tag{3.22}$$

Table 3.4 Measured Performance and Comparison with State of the Art

Ref.	Process (nm)	Supply (V)	BW (kHz)	SNDR (dB)	SNR (dB)	DR (dB)	***Power (μW)	FOM$_{SNDR}$ (pJ/conversion)	FOM$_{DR}$ (dB)
2005 [18]*	350	0.6	24	77	77	78	1000	3.6	151.8
2008 [20]**	130	0.9	20	73.1	82.2	83	60	0.406	168.22
2009 [66]**	180	0.7	20	81	84	85	36	0.098	172.44
2009 [15]**	180	0.7	25	95	100	100	2160	1.174	169.66
2010 [19]**	180	1	20	84	87	88	860	1.66	161.66
2012 [16]**	130	0.5	20	81.7	82.4	85	35.2	0.088	172.54
2012 [77]**	180	1	16	91.3	NA	93	190	0.197	172.25
2013 [55]**	1.2	130	20	72.5	74.7	83	165	1.19	163.8
2013 [67]*	65	0.8	20	91	94	98	230	0.198	177.39
2013 [56]**	180	1.8	10	84	84.4	88	155	0.59	166.09
2013 [5]**	130	1.2	10	87.8	89.2	90	148	0.368	168.29
2015 [78]*	130	0.4	20	76.1	77.7	82	63	0.301	167.01
2016 [71]*	180	1.8	20	97.7	98.6	100.5	300	0.12	178.73
This work*	180	0.9	20	86.4	88.7	91	103.4	0.15	173.86

* SC MASH structure, ** SC single-loop structure, *** Power consumption of the decimation filter is excluded for all design

The $\Delta\Sigma$Ms presented in [67] and [71] achieve 3.5-dB and 4.8-dB better FOM$_{DR}$ than this work at the expense of about 2.2 and 3 times the power consumption, respectively while the first one is a single-bit MASH 2–1 and the latter is a single-bit single-loop third order $\Delta\Sigma$M. Moreover, the worst case PSRR is the positive PSRR for a 2% mismatch of NMOS transistors in the proposed SBB inverter-based OTA. Nonetheless, the proposed SBB inverter-based OTA shows 12-dB improvement compared to that proposed in [67]. Although, there is a similarity between the OTA designed in the proposed work to that presented in [55], the inverter-based OTAs used in the proposed design are biased in weak-inversion, resulting in lower thermal noise and power consumption. Moreover, the proposed SBB inverter-based OTA meets the specifications at the SS process corner as well as low supply voltage. Gain-boosted technique is utilized in [67] at the expense of added power consumption and circuit complexity. However, it is shown that the proposed topology needs only 50-dB OTA DC-gain and it is met by the proposed SBB inverter-based OTA. Therefor, neither gain-boosting technique nor complex PVT compensation techniques are required. Modifying the proposed topology to that presented in [61], could help to lower the OTA DC-gain. In that case, the modulator in [61] is re-analyzed for an OSR of 128 and it is observed that a 20-dB OTA DC-gain is sufficient to keep IBN$_{max}$ intact, outlining a potential improvement strategy to attain a lower critical OTA gain value. This architecture also shows better linearity hence potentially allowing for an improvement in DR. Finally, the $\Delta\Sigma$M proposed in [16] shows a

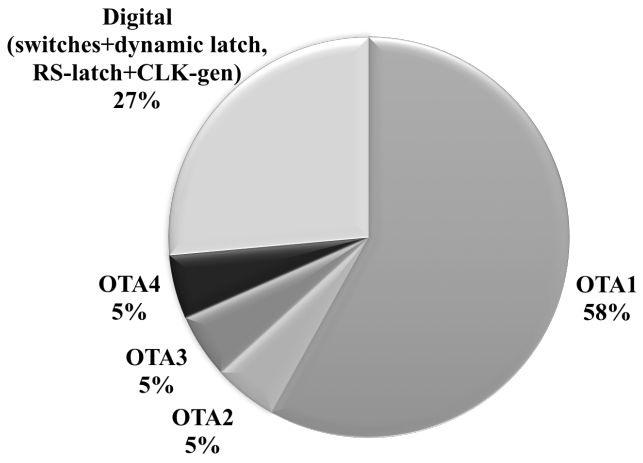


Figure 3.22 Power consumed by the different ΔΣM building blocks.

better power efficiency, however, it is essentially due to the lower supply voltage leading to somewhat reduced DR.

3.9 Conclusion

A 20-kHz signal bandwidth ΔΣM is described in this paper. The adder block is eliminated in the conventional second order FF ΔΣM by moving the adder back to the input of the second integrator. The second integrator hence acts as an integrator and as an adder, simultaneously. It is shown that the quantization error can be extracted by proper combination of three analog signals : i.e. the input signal, and the outputs of the first and second integrators. Such an error extraction makes the proposed adder-less topology well-suited for applications requiring multi-bit quantizer. The quantization error is fed to another adder-less topology to form a MASH 2-2 ΔΣM. A SBB inverter-based OTA, biased in the weak-inversion, is proposed to realize the integrators, resulting in lower thermal noise compared to that of presented in [55]. Slow process corner and low V_{DD} failure is mitigated by the bulk biasing technique. The circuit is fabricated in 0.18-μm CMOS technology. The prototype achieves a SNR, SNDR and DR of 88.7 dB, 86.4 dB and 91 dB, respectively. The circuit consumes 103.4-μW at a 0.9-V supply voltage, exhibiting a cutting-edge performance in comparison to the state of the art.

CHAPTER 4 ARTICLE 2 : SMASH ΔΣ MODULATOR WITH ADDERLESS FEED-FORWARD LOOP FILTER

4.1 Overview

One of the main bottlenecks in a MASH ΔΣM is the SNDR degradation due to mismatches between analog coefficients and the digital cancellation logic. SMASH topology is a promising approach to overcome this issue. A modified SMASH topology is proposed in this chapter. The following sections are the reproduction of an accepted article in Electronics Letters.

— Article 2 : M. Honarparvar, J. M. de la Rosa, F. Nabki and M. Sawan, "SMASH ΔΣ modulator with adderless feed-forward loop filter," in Electronics Letters, vol. 53, no. 8, pp. 532-534, 13 4 2017 [61].

4.2 Abstract

A novel cascade ΔΣ modulator, which combines the benefits of SMASH topology and feed-forward loop filter, is presented in this letter. The proposed ΔΣ architecture is based on moving the power-hungry adder block from the quantizer input to the first integrator output. The proposed architecture shows a better OTA linearity and relaxed OTA DC-gain compared to conventional MASH and SMASH topologies. This feature makes the modulator topology more suitable than conventional MASH and SMASH topologies for low-voltage applications.

4.3 Introduction

Delta sigma modulators (ΔΣMs) are widely used in low-power high-speed applications. Due to low oversampling ratio (OSR) in high bandwidth applications, higher order modulators can be used to meet the dynamic range (DR) requirement. However, the use of higher-order loop filter makes a ΔΣM severely susceptible to instability. Although employing MASH structure guarantees stable operation, it needs high-gain and power-consuming operational transconductance amplifier (OTA), used in the integrators, to minimize the quantization error leakage due to analog and digital filter mismatches. The sturdy MASH (SMASH) structure has been published [79], and depicted in Fig. 4.1, in which the first stage quantization error is noise-shaped instated of canceling the error, to obviate the matching requirements. However, the modulator presented in [79] suffers from two drawbacks. First, a highly linear digital-to-analog converter (DAC) is required in the added feedback path to the first stage input.

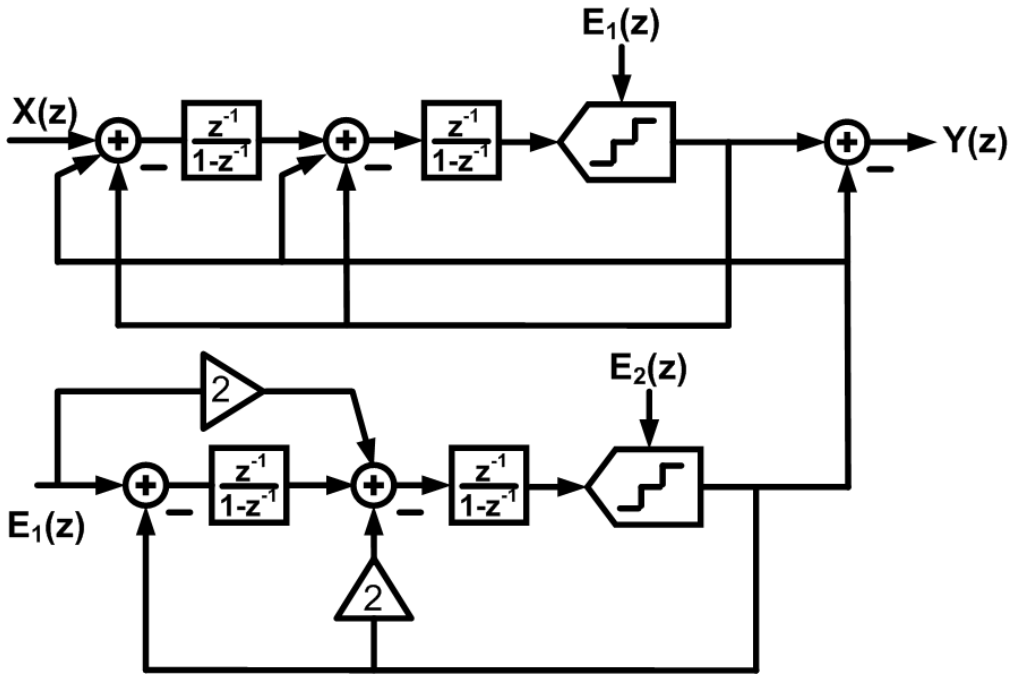


Figure 4.1 Block diagram of the conventional SMASH architecture [79]

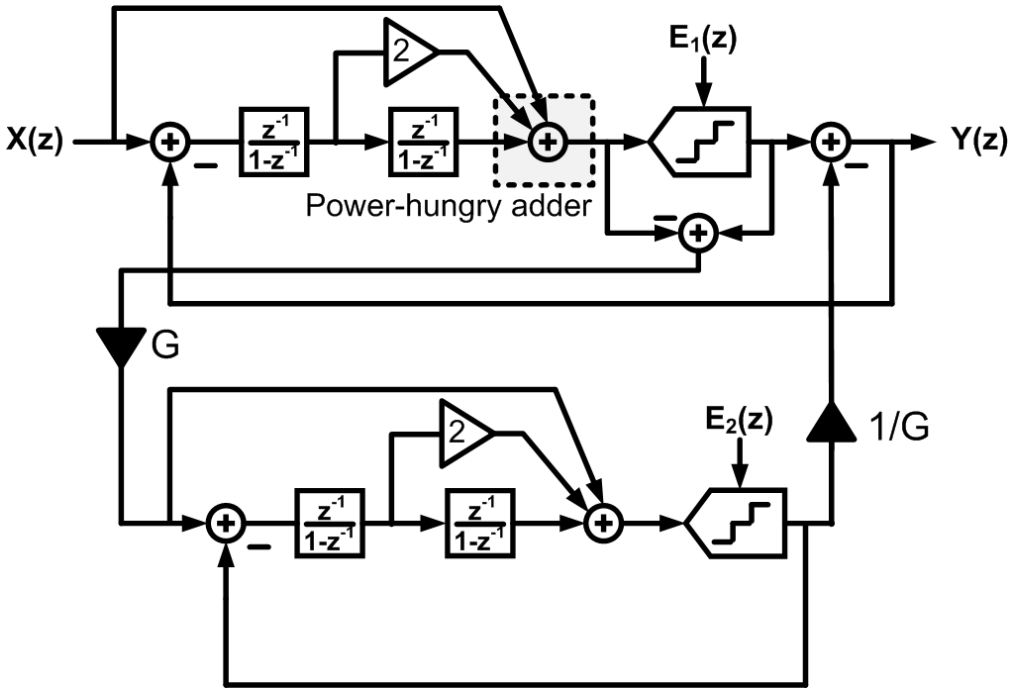


Figure 4.2 Block diagram of the modified SMASH [80]

Second, added feedback paths are sensitive to mismatch, which causes low-order quantization noise leakage. To circumvent these two drawbacks, an improved SMASH $\Delta\Sigma$M, shown in

Fig. 4.2, has been introduced in which a unity signal transfer function (STF) topology was utilized [80]. The main problem of the $\Delta\Sigma$M in Fig. 4.2 is that a relatively high-speed active adder is needed at the input of the quantizer and it consumes power. It is worth noting that although a passive adder consumes much less power, it is not suitable as it capacitively loads the second integrator. This increased loading results in more stringent requirements on the second integrator.

To overcome the aforementioned drawbacks, a cascade $\Delta\Sigma$M with modified unity STF feed-forward architecture [59] for low-power high-speed application is addressed in this letter. The main features of the proposed modulator are the following. First, the high-speed and power-hungry adder in front of the quantizer is removed and the preceding integrator performs this task. Second, the STF of the proposed modulator is modified to unity i.e. $STF = 1$. Third, taking the advantage of the SMASH topology, quantization error is canceled in the proposed architecture and fourth, the number of feedback DACs is less than what has been proposed in [79].

4.4 Proposed SMASH topology

The proposed modulator is illustrated in Fig. 4.3. The following strategies are used to overcome the drawbacks of two previous modulators.

— The summation block is moved back to the input of the second integrator, thus resulting in the addition operation being performed at the input of the second integrator. Therefore, the high-speed power-hungry adder is no longer needed.

— The STF of the modulator is restored to unity by inserting a direct feed-forward from the input of the modulator to the input of the second integrator with the transfer function of $1 - z^{-1}$. Having had the first stage of the proposed modulator, the NTF and STF of the first stage itself can be expressed as follows,

$$Y_{1st-stage}(z) = STF_1.X(z) + NTF_1.E_1(z) \tag{4.1}$$

where $X(z)$ is the input signal, $STF_1 = 1$, $NTF_1 = (1 - z^{-1})^2$ and $E_1(z)$ stands for the quantization error of the first stage.

— Feedback paths from the second stage to the first one are omitted by inserting the modulator output back to the first stage input, and output bitstreams of both stages are digitally subtracted inside the loop filter of the first stage. Hence, the number of feedback DACs is less than the modulator proposed in [79].

Note that, contrary to the conventional SMASH $\Delta\Sigma$M, the quantization error of the first

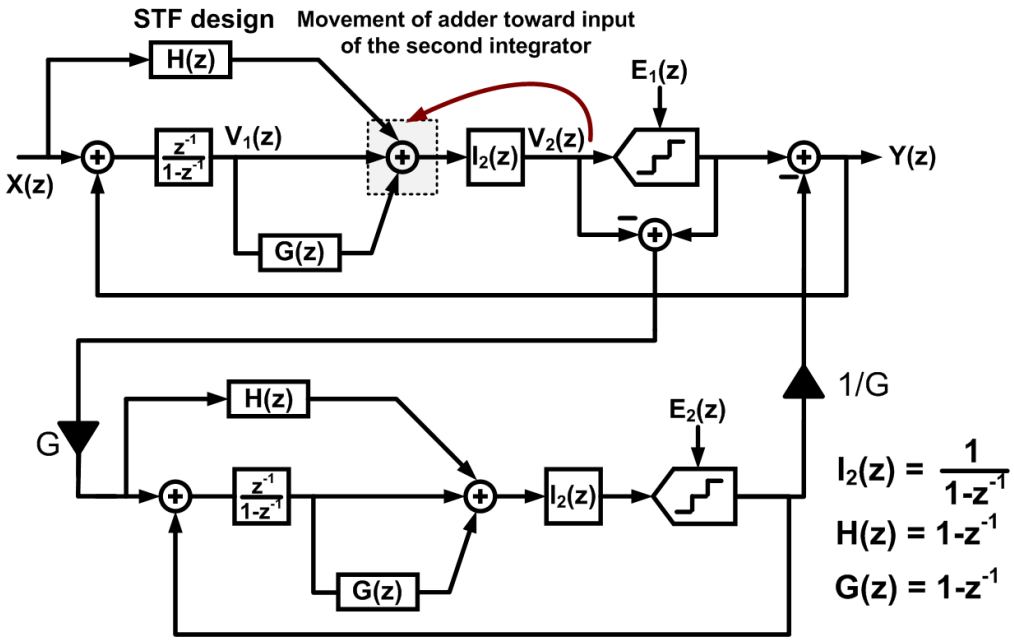


Figure 4.3 Block diagram of proposed adderless SMASH ΔΣM

stage is completely canceled without using any digital cancellation logic. Moreover, using interstage gain (denoted as G in Fig. 4.3) would not be effective in the conventional SMASH since $E_1(z)$ is not completely canceled out, and as a consequence further reduction of the $E_2(z)$ would not improve the noise suppression significantly. However, this drawback is solved in the proposed modulator. Having had above descriptions and using a linear model for the quantizers, the Z-domain transform of the modulator output is expressed by :

$$Y_{proposed-SMASH}(z) = X(z) - \frac{1}{G}(1 - z^{-1})^4 . E_2(z) \tag{4.2}$$

where $X(z)$ is the input signal, G stands for the interstage gain and $E_2(z)$ is the quantization error of the second stage.

4.5 Simulation results

For comparison purposes, both conventional MASH 2-2 ΔΣM and conventional SMASH 2-2 ΔΣM as well as proposed architecture are simulated by using MATLAB/SIMULINK. For all simulations, a 4-bit quantizer, $OSR = 8$ and 1-V reference voltage are considered. The OTA DC-gain requirement of the above-mentioned structures is illustrated in Fig. 4.4. It is shown that the proposed ΔΣM is more robust in terms of finite OTA DC-gain. Note that the conventional MASH structure needs an OTA with the DC-gain of at least 40-dB to avoid the

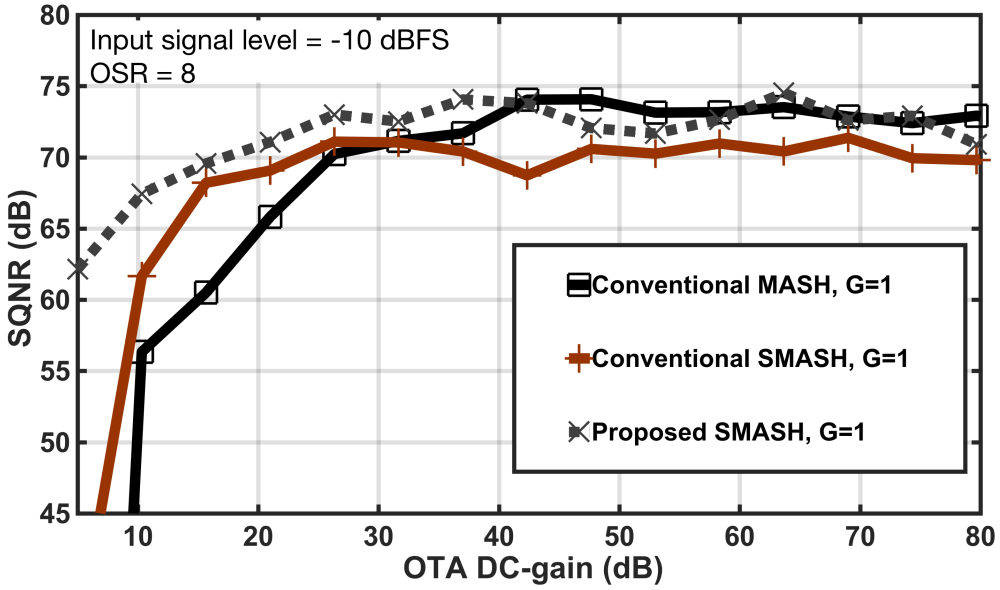


Figure 4.4 SQNR versus OTA DC-gain

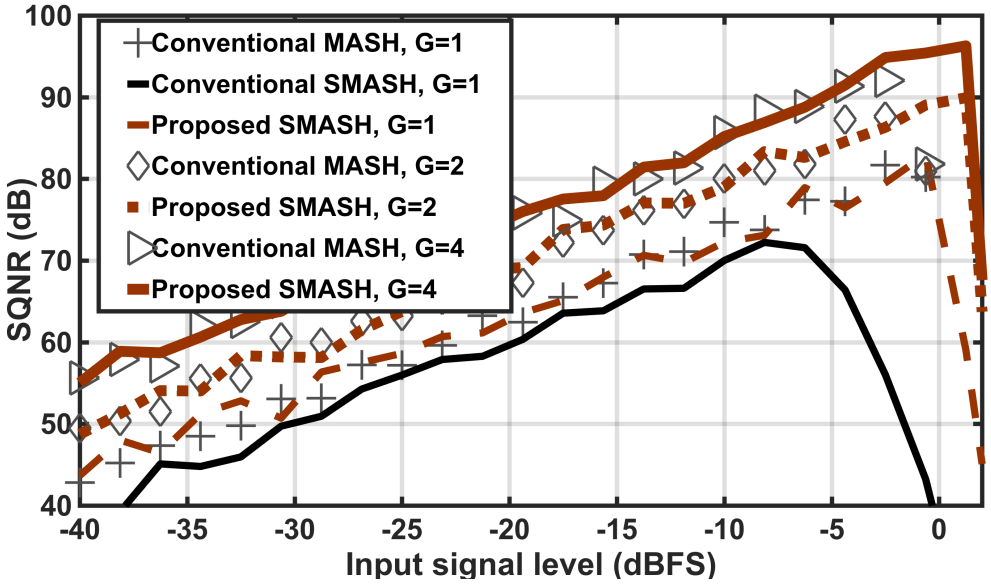


Figure 4.5 SQNR versus input signal level

signal to quantization noise ratio ($SQNR$) degradation from the maximum value, while the proposed architecture requires less than 20-dB OTA DC-gain. It is also worth noting that the $SQNR$ drastically drops below this value in a conventional SMASH topology.

Fig. 4.5 shows the $SQNR$ versus input signal level by comparing the conventional MASH and SMASH architectures with the proposed $\Delta\Sigma$M with $G = 1, 2$ and 4. An ideal (infinite)

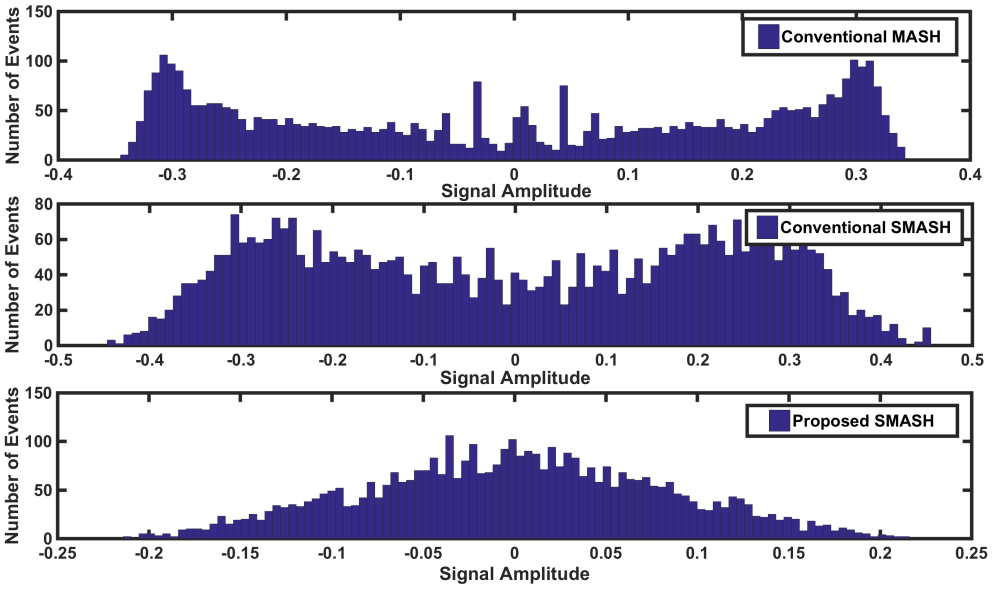


Figure 4.6 First integrator output histogram

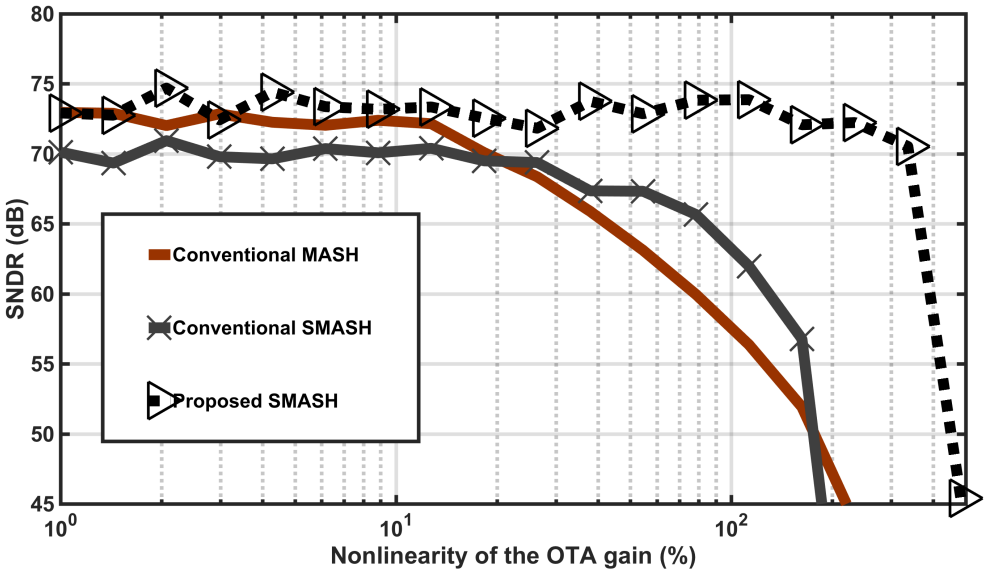


Figure 4.7 Effect of OTA nonlinearity on the SNDR

value of the OTA DC-gain is assumed for all cases. It is shown that the proposed modulator demonstrates better performance in terms of both maximum $SQNR$ and overload level. Moreover, the achievable maximum $SQNR$ can be increased by considering $G > 1$. The output histogram of the first integrator for all modulators is depicted in Fig. 4.6. It can be noted that the combination of unity STF and multi-bit quantizer results in a relaxation of the output swing for the proposed $\Delta\Sigma$M compared to conventional MASH and SMASH

topologies. This is very important in a limited voltage headroom implementation.

The proposed SMASH topology is also more robust against OTA nonlinear DC-gain. This is illustrated in Fig. 4.7, where the influence of the front-end integrator OTA nonlinearity is shown and compared with both conventional MASH and SMASH topologies, by considering a DC-gain of 50-dB and an input signal level of −10-dB below full-scale range (dBFS).

4.6 Conclusion

A new adderless SMASH ΔΣM based on a feed-forward loop filter is presented. The main bottleneck of the feed-forward topology i.e. high-speed power-hungry adder is mitigated by moving the adder back to the input of the second integrator. The STF of the proposed SMASH ΔΣM is restored to unity which makes the proposed architecture robust to OTA nonlinearity. Unlike the conventional SMASH structure, quantization error of the first stage is fully canceled in the proposed architecture. As a consequence, the interstage gain can now increase the performance of the proposed modulator. All above-mentioned characteristics make the proposed architecture suitable for low-voltage, low-power and high-speed applications.

CHAPTER 5 ARTICLE 3 : A 10-MHz BW 79.2-dB SNDR 640-MS/s CONTINUOUS-TIME FOURTH-ORDER MASH ΔΣ MODULATOR USING GRO-BASED QUANTIZATION

5.1 Overview

Time domain signal processing is a promising approach to realize analog and mixed signal building blocks without being concerned about voltage headroom. Analog and mixed signal building blocks can be either implemented in a pure time domain or a hybrid voltage and time domain. It is shown that the hybrid realization of a mixed mode circuit (a ΔΣM as an example) can help to take the advantages of both domains. The following sections are the reproduction of a submitted article to IEEE Transactions on Circuits and Systems-I : Regular Papers

— Article 3 : M. Honarparvar, J. M. de la Rosa, and M. Sawan, "A 10-MHz BW 79.2-dB SNDR 640-MS/s Continuous-Time Fourth-Order MASH ΔΣ Modulator Using GRO-based Quantization", Submitted IEEE Transactions on Circuits and Systems-I.

5.2 Abstract

This paper presents a novel multi-stage noise-shaping (MASH) 3-1 Continuous-Time (CT) Delta-Sigma Modulator (ΔΣM) with Gated Ring Oscillator based Quantizers (GROQs) in both stages of the cascade. Only two active-RC integrators – realized by self-biased inverter-based amplifiers – are needed to implement the loop filter, and the overall quantization noise-shaping is enhanced by the action of the implicit (first-order) filter provided by the embedded GROQs. The use of GROQs increases the linearity performance with respect to the conventional Voltage Controlled Oscillator based Quantizers (VCOQs) and allows a more robust extraction of the front-end stage quantization error in the time domain, thus making the proposed architecture more suitable to implement high-order expandable scaling-friendly cascade ΔΣMs, in which the back-end stages are implemented by mostly-digital GRO-based Time-to-Digital Converters (TDCs). The proposed circuit has been fabricated in a 65-nm CMOS technology with 1-V supply voltage. The chip prototype operates at 640-MHz sampling frequency to digitize 10-MHz signals. To the best of the authors' knowledge, this is the first reported experimental demonstration of a GRO-based CT MASH ΔΣM, featuring an 81.5-dB SNR at −2.2-dBFS, a 79.2-dB SNDR at −4-dBFS and a dynamic range (DR) of 80 dB, with a power consumption of 12-mW. These metrics demonstrate state-of-the-art

performance, with a Walden FOM of 80.5 fJ/conv-step and a Schreier FOM of 169.2 dB, thus demonstrating the benefits of the proposed GRO-based.

5.3 Introduction

Continuous-Time (CT) ΔΣ Modulators (ΔΣMs) have demonstrated to be the most efficient technique to implement Analog-to-Digital Converters (ADCs) in a number of applications requiring medium resolution (12-14 bit) within a signal BandWidth in the order of 10-100MHz [81]. At these speeds, the OverSampling Ratio (OSR) is limited by the prohibitive sampling rates – usually in the order of several GHz – while the loop-filter order cannot be increased beyond four or five due to stability constraints. Thus, multi-bit quantization is needed in many cases in order to meet the Dynamic Range (DR) requirements. However, the design of conventional amplitude-based (Flash) quantizers is severely conditioned by the reduction of supply voltages associated to technology downscaling [10].

These limitations have prompted the interest by the so-called time/frequency-based quantization rather than the conventional amplitude-based quantization. This way, as the digitized information is codified in time domain, the DR of the ADC is not so conditioned by the voltage headroom available to design analog and mixed-signal circuits – such as ΔΣMs in nanometer CMOS. One of the first successful implementations of time/frequency-based ADCs was proposed in [30], where the authors replaced the quantizer of a ΔΣM by a ring oscillator to count the number of edges within a given time period, so that a digital time-based representation of the input signal is obtained. Moreover, VCO-based quantizers provide an implicit first-order noise-shaping due to their inherent differentiator operation required to implement the frequency-to-voltage conversion in the digital domain. Moreover, VCOQs provide also implicit Dynamic Element Matching (DEM) when it is used as voltage-to-frequency (V-to-F) converter. These features have been exploited by ΔΣM designers to increase the noise-shaping filter order of ADCs, without increasing the order of the embedded analog filter, thus resulting in a mostly-digital/scaling-friendly circuit realization [21, 30, 82, 31, 83, 13, 84–91, 32, 37, 92]. However, the price to pay for using VCOQs is the nonlinearity associated to the V-to-F transfer characteristic [30], what has motivated the exploration of some alternatives – conceptually depicted in Fig. 5.1 – such as TDCQs or VCOs used as Voltage-to-Phase (V-to-P) converters [21, 30, 31, 13]. The latter improves the linearity of VCOQs at the expense of losing their inherent DEM [31]. Therefore, additional calibration or linearization techniques are required, which usually introduce extra loop delay and make the design of the modulator more complex and sensitive to instability.

Another solution to overcome the nonlinearity of VCOQs is to lower signal swing seen by

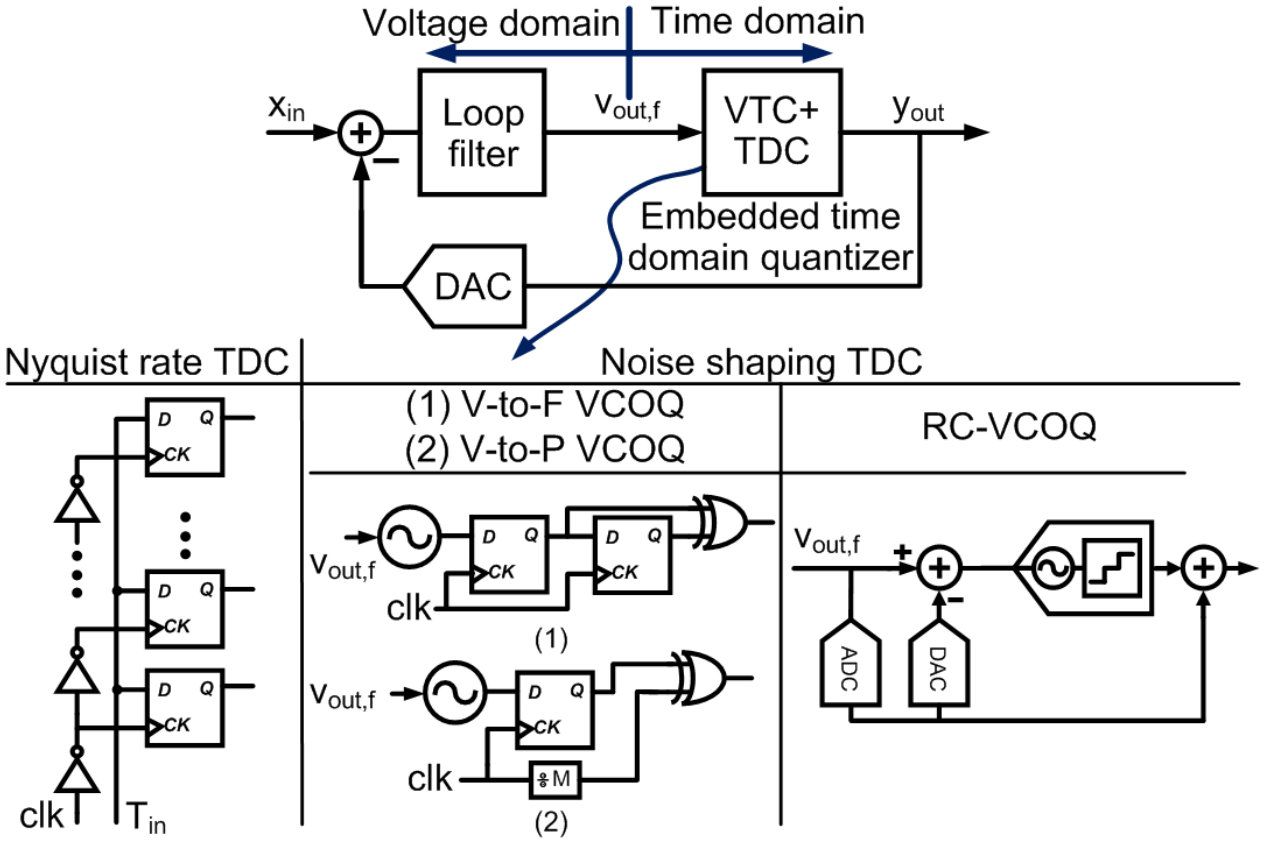
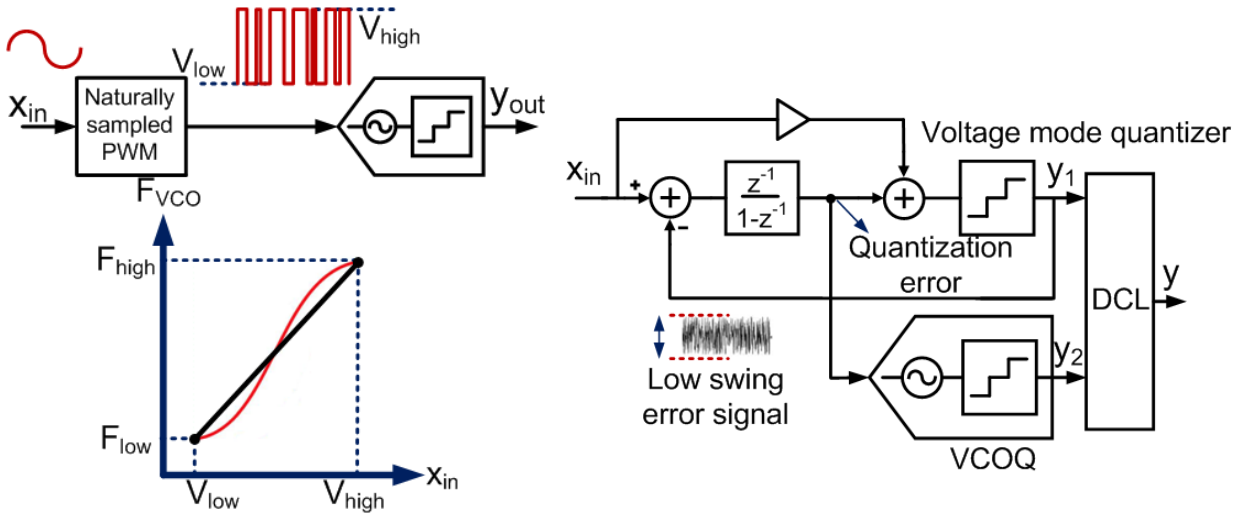


Figure 5.1 Conceptual block diagram of prior approaches to implement time/frequency-based quantizers in ΔΣMs : Nyquist rate TDC [21], V-to-F VCOQ [30], V-to-P VCOQ [31] and RC-VCOQ [13].

the VCO, so that the nonlinear tuning characteristic of the VCOQ is not exercised. This can be performed by subtracting the output of the VCOQ from its input to provide a residue signal and using the resulting residue either in a Residue Cancelling (RC) VCOQ based CT-ΔΣM [13] or a two-stage CT-ΔΣM [92]. Since the quantization error is not available in a VCOQ, both architectures require extra Digital-to-Analog Converters (DACs) and auxiliary calibration circuits to extract the quantization error.

An interesting approach to palliate the nonlinear behavior of VCOQs is to force them to operate over two points on the V-to-F transfer characteristic thanks to the action of a pulse width modulator (PWM) [41], as conceptually depicted in Fig. 5.2(a). However, the main drawback of such a solution is that the quantization error is difficult to extract in order to implement MASH ΔΣMs. Moreover, the non-linear characteristic of the PWM is not noise-shaped since it is directly injected to the input of the ADC. Alternatively, the VCO can be placed only in the back-end stages of MASH topologies as proposed by the authors in [53]



(a) (b)

Figure 5.2 Conceptual block diagram of prior approaches to implement VCOQ in an open-loop mode : (a) Naturally sampled PWM followed by a VCOQ to digitize the input signal [41], (b) VCOQ to digitize quantization noise in the back-end of a multi-rate MASH ΔΣM [53].

– conceptually shown in Fig. 5.2(b)– in which a first-order Discrete-Time (DT) single-loop ΔΣM is used in the front-end stage, which operates at a lower rate than the back-end VCOQ stage in a multi-rate configuration. Thus, the nonlinearity of the VCO is attenuated by the gain of the front-end stage, although the maximum speed of the converter is limited by the front-end DT filter.

Some of the mentioned limitations can be overcome by using the so-called Gated Ring Oscillators (GROs), where the oscillator is controlled by an enable signal, so that it oscillates when such a signal is high and freezes otherwise. Multi-bit quantization can also be implemented by using multi-path GROs [82, 50]. These kinds of time encoders have been embedded in a ΔΣ *error feedback structure*, as a MASH 1-3, in order to build TDCs [50]. However, this architecture severely suffers from the following drawbacks. First, the required Digital Cancellation Logic (DCL) is not effective when swapping the stages to configure a MASH 3-1 structure [50]. Second, the nonlinearity, caused by the voltage-to-time converter in the front-end stage, is directly added to the output of the first stage and hence degrading the performance of the TDC. Third, the phase-noise of the GRO, used in the front-end stage, severely deteriorates the overall performance of the TDC. The use of GROs have also been exploited by the authors in [93] to implement a single-loop fourth-order ΔΣM with a multi-bit time-encoded quantizer made up of two stages, in which the GRO is placed in the back-end stage, while the front-end stage is based on the so-called Noise-Shaped Integrated Quantizer (NSIQ).

However, although these approaches palliate the nonlinear problems of time-encoded quantizers to some extent, the price to pay in most cases is an increased circuitry complexity and its involved dynamics, what makes the resulted ADC more sensitive to timing errors, such as clock jitter error, thus reducing their potential use in high-speed applications. Moreover, the error extraction is also difficult to implement in cascade topologies using multi-bit quantization in both stages, which – to the best of the authors' knowledge – explains why this approach has not been successfully demonstrated experimentally in MASH ΔΣMs.

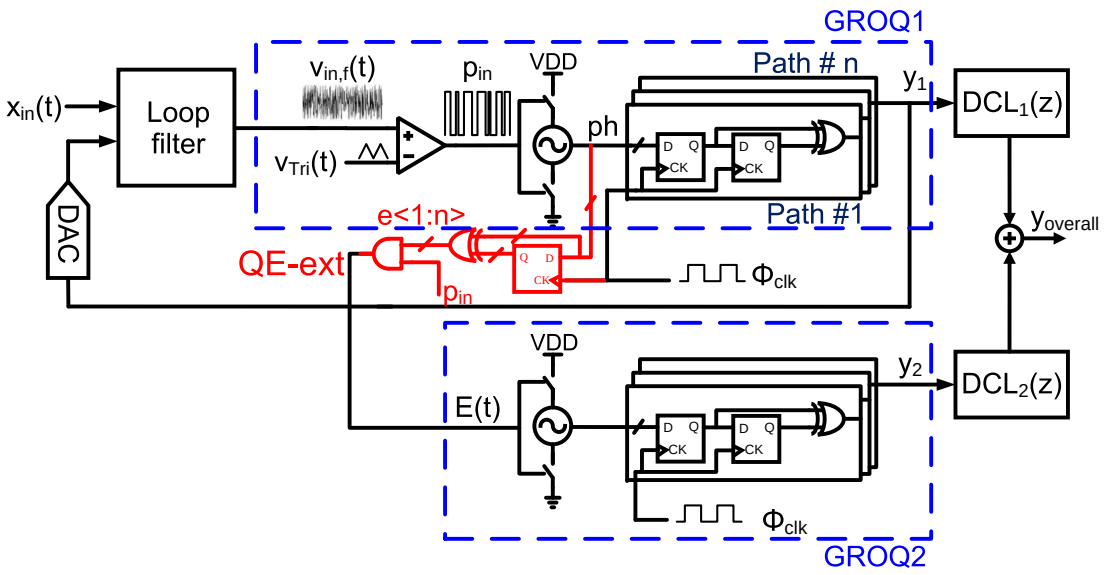
This paper contributes to this topic, and extends the idea presented in [94] for the implementation of CT MASH ΔΣMs with multi-bit GROQs in all stages. The time-based quantizer consists of a PWM followed by a GRO-based TDC. This strategy allows to extract the quantization error in a more robust way in order to build cascade topologies where the back-end stages are simple GRO-based TDCs, thus allowing to build high-order mostly-digital ΔΣMs. Compared with the architecture presented in [94], which is limited in practice by the transient response of the DT loop filter used in the front-end stage, the modulator presented in this paper embeds a GRO-based TDC in a CT MASH ΔΣM, thus benefiting from the combination of power-efficient CT loop filter and the inherent linearity of GRO-based quantization. Moreover, the quantization error of the front-end quantizer is extracted in time-domain, so that the back-end stages of the cascade can be implemented by GRO-based TDCs in a mostly-digital scaling-friendly way. That is an important feature, considering that the quantization error extraction is troublesome in voltage-mode CT MASH ΔΣMs as studied by the authors in [95]. In order to validate the proposed approach, a CT MASH 3-1 ΔΣM circuit has been designed to digitize 10-MHz signals with 80-dB DR. The chip has been fabricated in 65-nm CMOS technology, featuring state-of-the-art performance while demonstrating for the first time the benefits of embedding GRO-based quantizers in CT cascade ΔΣMs.

Following this introduction, the remaining of this paper is organized as follows. Section II describes the architecture and the high-level synthesis of the proposed modulator. The impact of main non-idealities is analyzed in Section III. Circuit design and simulated performance is presented in Section IV. Finally, experimental results are given in Section V and conclusions are drawn in Section VI.

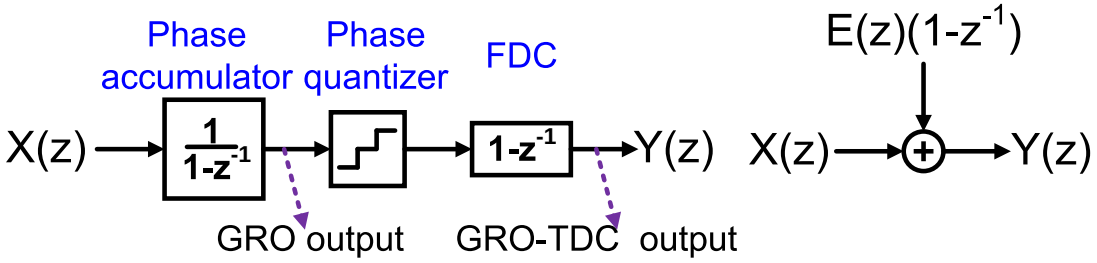
5.4 Proposed Modulator Architecture

Figure 5.3(a) shows the block diagram of the proposed GRO-based CT MASH ΔΣM. The front-end stage is made up of a CT filter, a multi-phase PWM-GROQ, and a feedback DAC [1],

1. An additional DAC – not shown for the sake of simplicity – is required to compensate the Excess Loop Delay (ELD).



(a)



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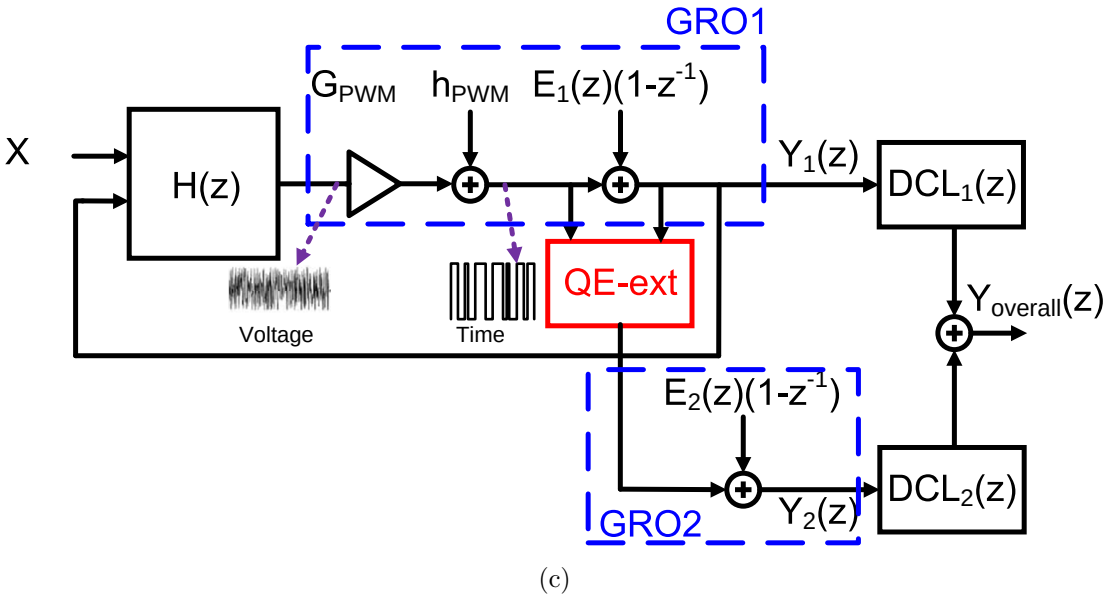


(c)

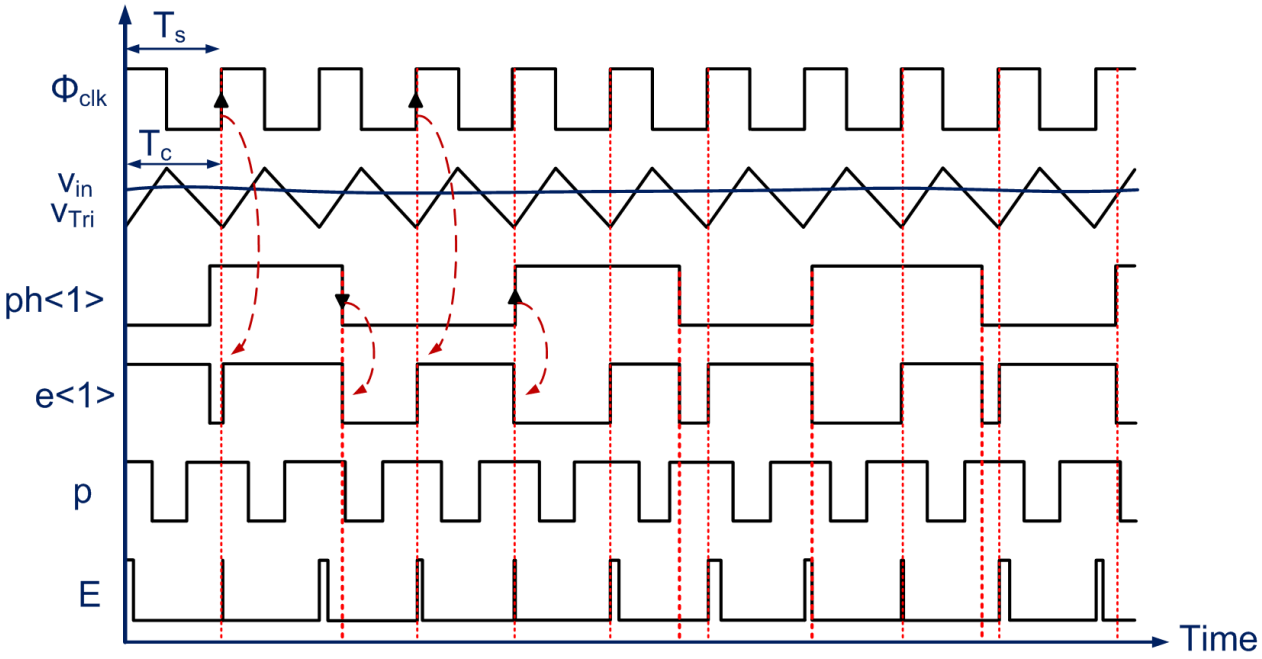
Figure 5.3 Proposed GROQ-based CT MASH ΔΣM : (a) block diagram, (b) DT representation of the GRO-TDC (left) and its equivalent linear model to synthesize the NTF (right) both showing an NTF of $(1 - z^{-1})$ and a STF of unity, (c) Linear model of the proposed modulator.

while the back-end stage is a multi-phase GRO TDC. The output voltage of the CT loop filter, $V_{\text{in,f}}(t)$, is compared with a triangle sinewave, $V_{\text{Tri}}(t)$, to generate a PWM signal, P_{in}, which controls the operation of the GRO, so that it oscillates when P_{in} is high or get frozen otherwise. Then, a counter generates a digital representation of the quantizer input by counting the output edges of the different GRO phases (ph) during a given sampling period, T_s=1/f_s, with f_s being the sampling frequency. A simple digital circuit, named QE-ext in Fig. 5.3(a), extracts the time-domain quantization error signal of the front-end stage quantizer, e $<$ 1 : n $>$ (with n being the number of phases), which in turns feeds the back-end stage and controls the operation of the GRO-TDC in this stage. The output of both stages are generated from their GRO outputs by using a Frequency-to-Digital Converter (FDC), which implements a differentiation transfer function by using D-type flip-flops and a XOR gate as shown in Fig. 5.3(a). Finally, the outputs of both stages, y_1 and y_2, are processed by the DCL functions, $\text{DCL}_i(z)$, in order to cancel out the front-end quantization error and to generate the overall modulator output, y_{overall}. Note that one of the key blocks in the proposed modulator is the quantization error extraction and generation– denoted as QE-ext in Fig. 5.3(c) – which allows to make CT MASH ΔΣMs more robust than using conventional (voltage-mode) quantizers as detailed below.

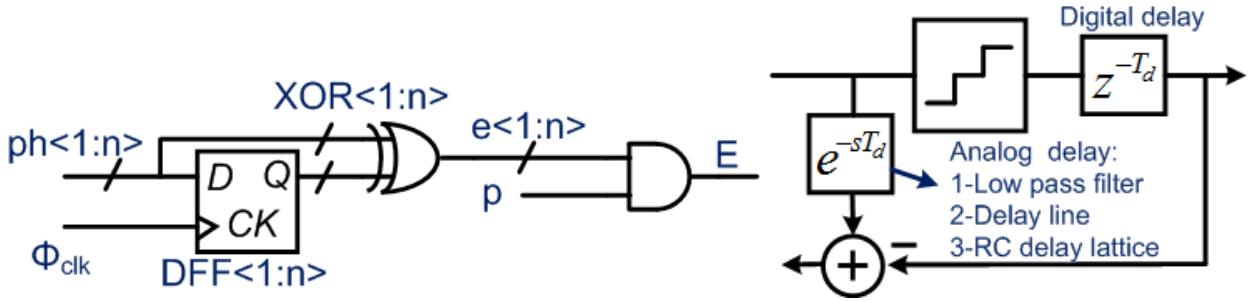
5.4.1 Time-based Quantization Error Extraction and Generation

The quantization error extraction in conventional CT MASH ΔΣMs with voltage-domain quantizers is an issue since they usually need to include a very well-controlled delay to properly determine the error and feed it to the next stage with the required synchronization [96, 95]. However, one of the benefits of the presented GROQ-based CT MASH ΔΣM is that the quantization error is available in the time domain and it can be extracted by a simple digital circuit, made up of a D-lach, a XOR gate and a NAND gate – as depicted in Fig. 5.3(a).

Figure 5.4(a) illustrates the mechanism of the quantization error extraction. As shown, the signal e$<$ n $>$ (n : number of phases in the GRO) is a pulse rises with the rising edge of the clock signal while its falling edge coincident with the closest rising/falling edge of the GRO phase, ph$<$ n $>$. All e$<$ n $>$s are then ANDed with the output signal of the PWM, p(t), resulting in final quantization error, E. Such an error is utilized to feed the back-end stage in the proposed CT MASH ΔΣM as shown in Fig. 5.3(a). The proposed quantization error generator for a multi-phase GRO is depicted in Fig. 5.4(b). In this circuit, an array of D-type flip-flops detects the rising edge of the clock signal and creates pulses when the rising/falling edge of the GRO phase appears. For comparison purposes, Fig. 5.4(c) shows the mechanism



(a)



(b) (c)

Figure 5.4 (a) Chronogram of the estimation of quantization error, (b) Proposed quantization error extractor, QE-ext (ph : output phase of the GRO, p : PWM pulse, E : quantization error and n : number of GRO phases), (c) Quantization error extraction in CT MASH ΔΣMs with voltage mode quantizer [96]-[97].

of the quantization error extraction in CT-ΔΣMs with voltage mode quantizer [96, 95, 97] while the analog delay is realized with an RC delay lattice in [95], a low-pass filter in [96], and a delay line in [97], result in a severely quantization noise leakage.

5.4.2 Linear Analysis of the Modulator

In order to analyze the proposed modulator, the linear models shown in Fig. 5.3(b)(c), are used. In this model, a DT loop filter is considered, and the PWM block is modeled by a gain, given by $G_{\mathrm{PWM}} = \frac{V_{\mathrm{DD}}}{V_{\mathrm{Tri}}}$ (where V_{DD} is the supply voltage and V_{Tri} is the peak-to-peak

carrier frequency of the PWM), and an additive harmonic distortion source in the front-end stage [2], represented by h_{PWM} [98]. The GRO TDCs in both stages are modeled as a DT differentiator, $(1 - z^{-1})$, with an additive time-based quantization error, E_i $(i = 1, 2)$, as shown in Fig. 5.3(b) [50].

Analyzing the linear model in Fig. 5.3(c), it can be shown that the Z-transform of the output of the front-end stage is given by :

$$\begin{aligned} Y_1(z) &= X(z) \cdot STF_1(z) \\ &+(E_1(z) \cdot (1 - z^{-1}) + h_{\mathrm{PWM}}) \cdot NTF_1(z) \end{aligned} \tag{5.1}$$

where $STF_1(z) = \frac{G_{\mathrm{PWM}} \cdot H(z)}{1+H(z)}$ and $NTF_1(z) = \frac{1}{1+H(z)}$ are signal transfer function (STF) and noise transfer function (NTF), respectively. As expected, the use of GROQs increases by one the order of noise-shaping with respect to that provided by the loop filter, $H(z)$, while the harmonic distortion associated to the PWM generator is also shaped by NTF_1.

The Z-transform of the output of the back-end stage is given by :

$$Y_2(z) = E_1(z) \cdot STF_2(z) + E_2(z) \cdot (1 - z^{-1}) \tag{5.2}$$

where $STF_2(z)$ is the STF of the back-end stage and it is considered as unity to simplify the analysis according to Fig. 5.3(b).

Assuming that $DCL_1(z) = STF_2(z)$ and $DCL_2(z) = NTF_1(z) \cdot (1 - z^{-1})$, it can be derived from (5.1) and (5.2) that the Z-transform of the overall modulator output is given by :

$$\begin{aligned} Y_{\mathrm{overall}}(z) &= X(z) \cdot STF_1(z) \cdot STF_2(z) \\ &+h_{\mathrm{PWM}} \cdot NTF_1(z) \cdot STF_2(z) \\ &+E_2(z) \cdot (1 - z^{-1})^2 \cdot NTF_1(z) \end{aligned} \tag{5.3}$$

From (5.3), it is inferred that the harmonics arising from the PWM are noise-shaped by the NTF determined by $H(z)$. On the other hand, the quantization error of the front-end stage is ideally cancelled out at the output and the quantization noise of the second stage noise is shaped by an overall NTF given by $H(z)$ and the second-order filtering provided by the two GRO-TDCs in the cascade.

Note that the back-end GRO-TDC helps to configure the modulator as a MASH structure

2. The back-end harmonic distortion associated to the PWM can be neglected since the input to this stage is the quantization error of the front-end stage, which is essentially a PWM (noisy) signal which does not generate any significant harmonic distortion.

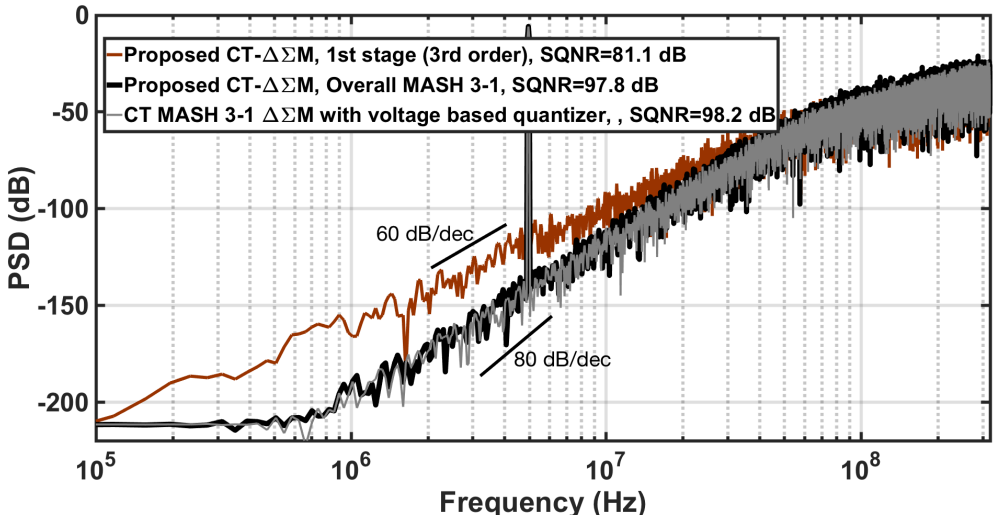


Figure 5.5 Simulated PSD of the proposed ΔΣM.

while this block cannot be performed by a VCOQ. This is due to the fact that the VCOQ must avoid an off state for the lowest frequency because if the front-end VCOQ is fully stopped, the quantization error becomes a DC value, and hence, this error prohibits the integrating operation of the second VCOQ in the back-end stage [99, 94]. Moreover, if a VCOQ is used, instead of a GRO-TDC, on one hand, an additional DAC would be required to extract the CT amplitude-based error signal and on the other hand the second VCOQ in the second stage would have to operate in a CT mode, and the non-linearity problem of the second VCOQ would be unavoidable.

5.4.3 DT-to-CT Transformation and Ideal Performance

As a case study, the proposed modulator has been synthesized to achieve a target SNDR of 80-dB within a signal bandwidth of 10-MHz. In order to get these requirements extensive behavioral simulations have been carried out in order to determine the optimum set of modulator system-level parameters, including the overall loop filter order, L, number of bits of the embedded quantizer, B, and OverSampling Ratio (OSR). Based on this study, the required ideal performance can be achieved with a fourth-order ($L = 4$) NTF, $B = 3$, OSR= 32 and an out-of-band gain, $H_{inf} = 1.5$. Taking into account these system-level parameters, the Schreier's toolbox is used to obtain the ideal NTF, yielding :

$$NTF_{\text{Ideal}}(z) = \frac{(z-1)^2}{(z^2 - 1.225z + 0.4415)} \tag{5.4}$$

As stated above, the effect of ELD is not considered at this step of the design process. In

order to compensate for this effect, an additional feedback DAC with adjustable gain – as proposed in [100]– will be used in the front-end stage as discussed later.

Once the overall ideal NTF has been obtained, the equivalent CT loop-filter can be obtained by applying the impulse invariant transformation method, yielding :

$$H_{\text{Loop}}(s) = \frac{0.22 \cdot f_s \cdot s + 0.054 \cdot f_s^2 \cdot}{s^2} \tag{5.5}$$

As an illustration, Fig. 5.5 shows the ideal Power Spectral Density (PSD) considering a half-scale input sinewave. This simulation has been obtained considering that the CT loop filter is modeled as an ideal RC filter and pseudo-differential 7-phase (ph = 7) GROs –which is equivalent to 3-bit quantization. The oscillation frequency is set to $f_{\text{GRO}} = \frac{f_s}{2}$ [30] and the carrier frequency of the PWM is set to f_s in order to minimize the effect of inter-modulation components.

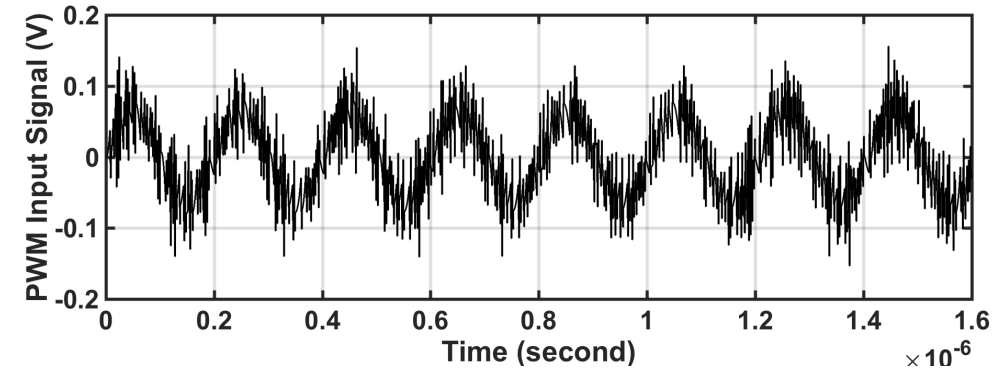
Note from Fig. 5.5 that a third-order and fourth-order noise-shaping with an SQNR of 81.1-dB and 97.8-dB for the front-end stage and the overall modulator are obtained, respectively. Thus, it can be concluded from Fig. 5.5 that the ideal performance of the presented by the proposed modulator is in a good agreement with what would be expected from an ideal conventional (voltage-domain) 3-bit CT MASH 3-1 $\Delta\Sigma$M.

5.5 Effect of Main Non-idealities

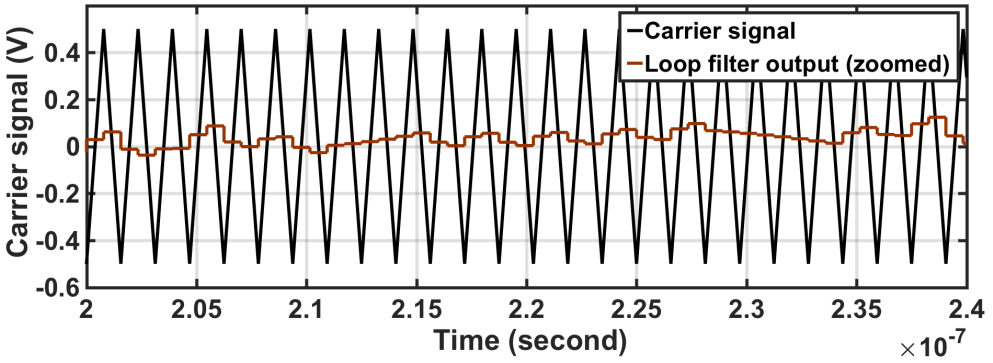
The analysis and performance shown in previous section considered that the proposed modulator is implemented by considering ideal building blocks. Such an ideal performance is degraded in practice by the effect of some circuits and systems error mechanisms, which need to be analyzed in order to optimize the design.

5.5.1 Modulation depth and inter-modulation harmonics

Two important limiting factors caused by the PWM generator as the modulation depth and the associated inter-modulation harmonic distortion caused by the mixed signal processing affecting the output of the modulator loop filter and the carrier signal. As an illustration, the loop-filter output as well as the PWM carrier signal are depicted in Fig. 5.6. The *modulation depth* – defined as the ratio between input signal of the PWM and triangle carrier signal– is less than 100% in practice. Note that this phenomenon is inherent to the PWM generation and it happens even so the comparator and the carrier signal are ideal. Indeed, the PWM behaves linearly as long as the modulation depth is less than 100%. However, there is another



(a)



(b)

Figure 5.6 (a) Loop-filter output signal of the proposed CT-ΔΣM, (b) PWM carrier signal and loop-filter output signal (zoomed).

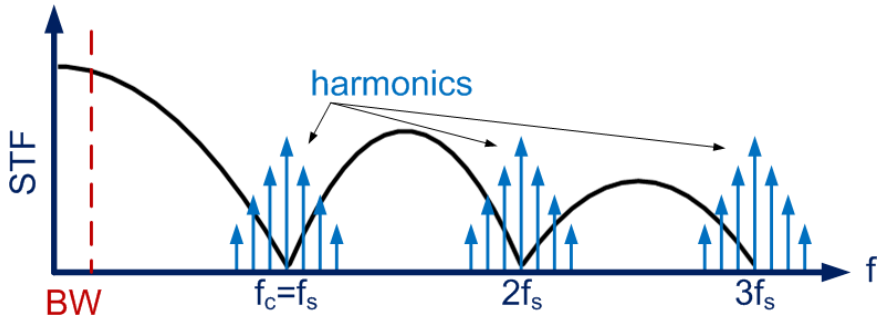


Figure 5.7 PWM harmonics filtered by the sinc function.

limitation associated with the modulation process and this limitation has nothing to do with the signal amplitude but with the carrier frequency of the PWM, i.e. f_c. The fact is that in the modulation process, the input signal and a set of sideband components can fall into the desired bandwidth and limit the resolution of the quantizer if f_c is not selected properly. As illustrated in Fig. 5.7, the STF of the GRO-TDC shows a sinc function nulling at αf_s with α being an integer number. It is therefore concluded that a great percentage of the sideband

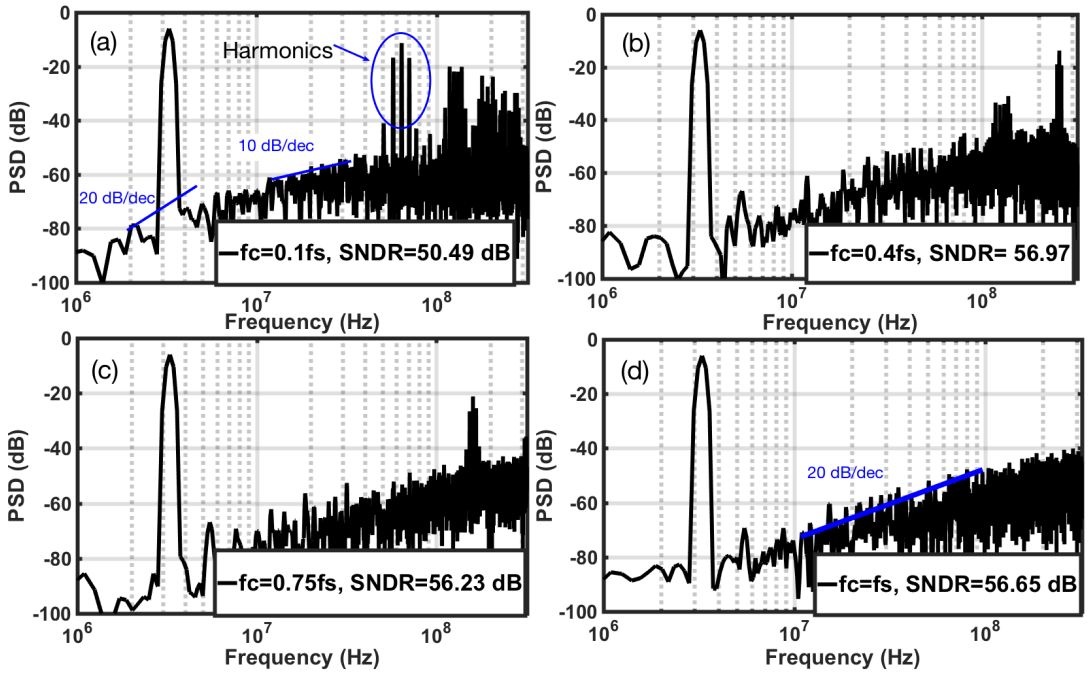


Figure 5.8 PSD and SNDR of a GRO-TDC for different carrier frequencies, (a) f_c=0.1f_s, (b) f_c=0.4f_s, (c) f_c=0.75f_s, (d) f_c=f_s.

components can be suppressed if f_c=f_s. However, it is a great of interest to decrease the carrier frequency of the PWM and hence the switching and the power consumption as well. To examine this effect, a Verilog-A simulation is carried out in which the power spectral density (PSD) of a GRO-TDC is plotted for various carrier frequencies, i.e. f_c=0.1f_s, 0.4f_s, 0.75f_s, f_s, as shown in Fig. 5.8. In this simulation, an input signal of −6 dBFS, a sampling frequency of 640 MHz over a bandwidth of 10 MHz is considered. The supply voltage of the comparator is 1 V and the peak-to-peak value of the PWM is set to 1 V as well resulting in a gain of 0 dB for the PWM. Fig. 5.8 shows an SNDR degradation of about 6 dB when setting f_c=0.1f_s compared to that of f_c=f_s. The harmonics also appear at that frequency. Moreover, the slope of the PSD at higher frequency is slightly lower than 20-dB/dec. However, a great amount of harmonics' energy is suppressed when f_c=f_s and the slope of 20-dB/dec is preserved at the higher frequencies. Based on these considerations, f_c=f_s is selected in this design.

5.5.2 Mismatch of GROs' Frequencies

Another source of error that need to be taken into account in the proposed modulator is caused by the mismatch between the GROs. This error causes a difference between the oscillating frequencies, and as a consequence, the first-stage quantization error cannot be

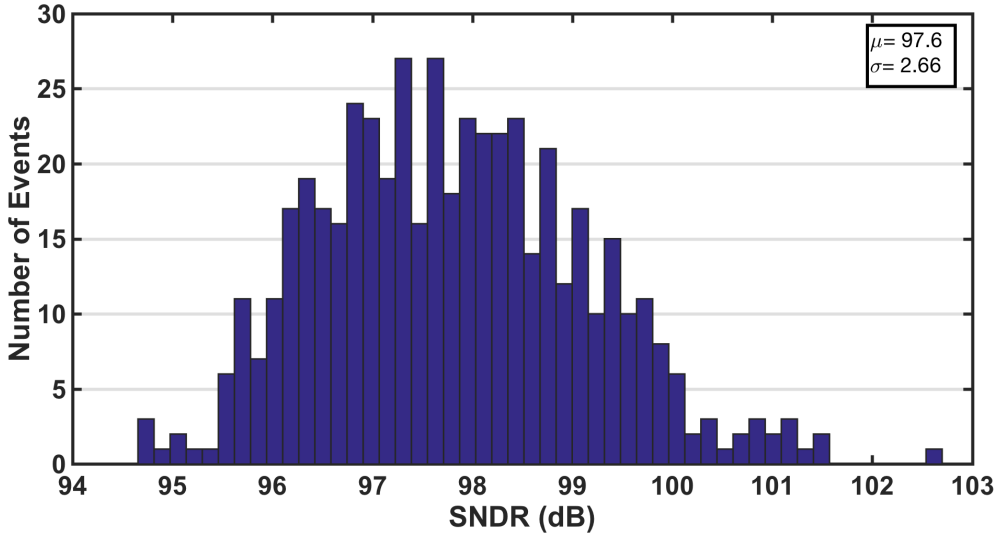


Figure 5.9 Effect of 10% frequency mismatch between the GROs' for the proposed modulator.

completely removed. To examine this effect, a 500-run Monte Carlo analysis was carried out for a 10% frequency mismatch. As depicted in Fig. 5.9, a deviation of about 3-dB in SNDR is observed while having a negligible distribution between 94-96 dB SNDR. Either careful layout design or forming a frequency-locked loop around the GROs could be the alternatives to mitigate this effect [50].

5.5.3 Phase Noise of GROs

Another error mechanisms associated to VCOs and GROs is the phase noise, which may also degrade the performance of the propose modulator by increasing the in-band noise power. The circuit elements, used to realize the oscillator, generate electrical noise and such noise is modulated by the oscillator resulting in spectrum contamination at the output of the oscillator around the oscillator frequency components. The FDC used in the GRO-TDC down-converts such a noise which appears at the output of the modulator. In order to analyze the effect of this error, the phase noise of GROs is extracted from electrical (transistor-level) simulations in the target technology (65-nm CMOS), obtaining phase noises of -106 dBc/Hz at 1-MHz offset. As depicted in Fig. 5.10, no degradation is observed for these phase-noise sources in the overall performance of the modulator. Such simulations are repeated by extracting different phase noise spectra and injecting the resulted phase noises into the behavioral model. As can be observed in Fig. 5.10, the proposed CT-$\Delta\Sigma$M is robust with respect to the GROs' phase-noise such that the proposed modulator maintains its performance for a phase-noise of -85 dBc/Hz at 1-MHz offset. An oscillator with a phase-noise of -43 dBc/Hz at 1-MHz

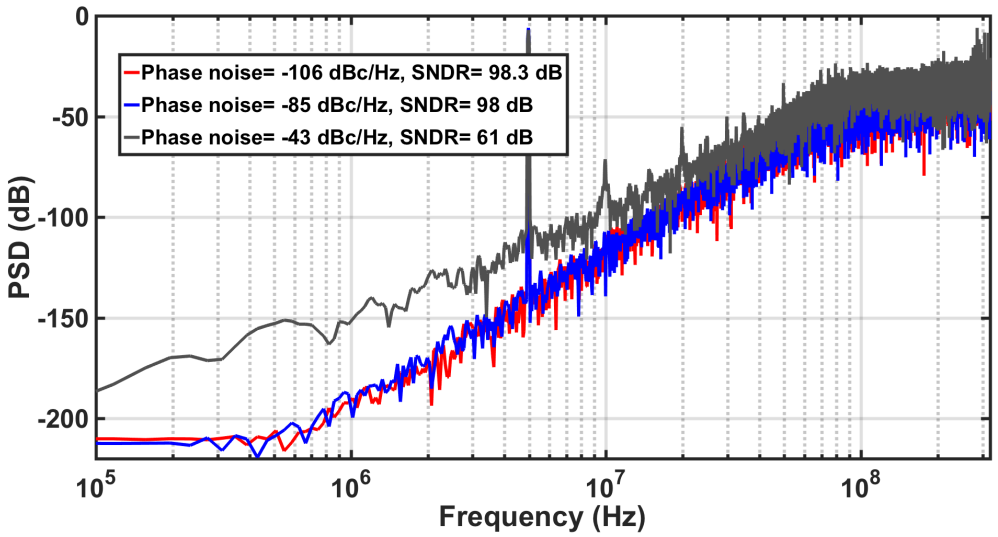


Figure 5.10 Effect of GROs' phase noise, all simulated at 1-MHz offset frequency, on the modulator performance.

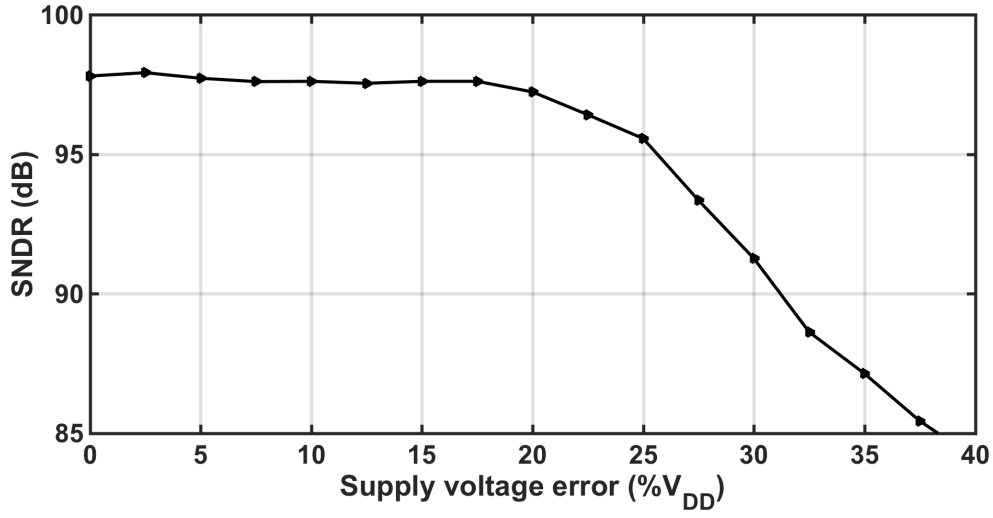
offset is employed in the proposed CT-ΔΣM. The SNDR severely levels off to 61-dB. Such a robustness is due to the fact that the phase-noise of the front-end stage is noise shaped by the loop-filter and the phase-noise of the back-end stage has a negligible impact on the overall performance as it is filtered out by the DCL_2. Consequently, unlike the data converter proposed in [50] where the phase-noise of the front-end stage deteriorates the performance of the overall modulator, a low-noise GRO is not required for the proposed CT-ΔΣM.

5.5.4 Supply voltage error

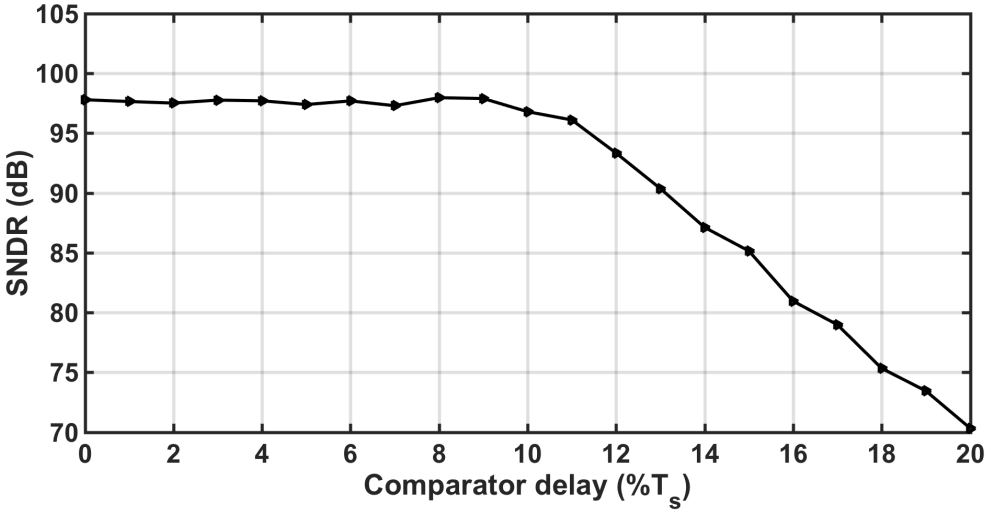
Any ripple in the supply voltage translates into a tone at the ripple frequency harmonics due to the modulation. Supply voltage error has low-frequency components around 50-Hz. A behavioral simulation is carried out to examine the effect of supply-voltage error in the PWM generator of the proposed CT-ΔΣM. As shown in Fig. 5.11(a), the modulator can tolerate up to about 20% ripple in the supply voltage. Beyond that value, the SNDR tends to be degraded such that a 30% ripple in the supply voltage results in a degradation of about 7-dB in SNDR. The proposed ΔΣM relies on the external low dropout (LDO) voltage regulators which provide clean supply voltages to the modulator.

5.5.5 Comparator delay

Comparator delay must be carefully addressed in the proposed ΔΣM since it can result in a phase shift leading to an unstable modulator. It is worth noting that if the comparator



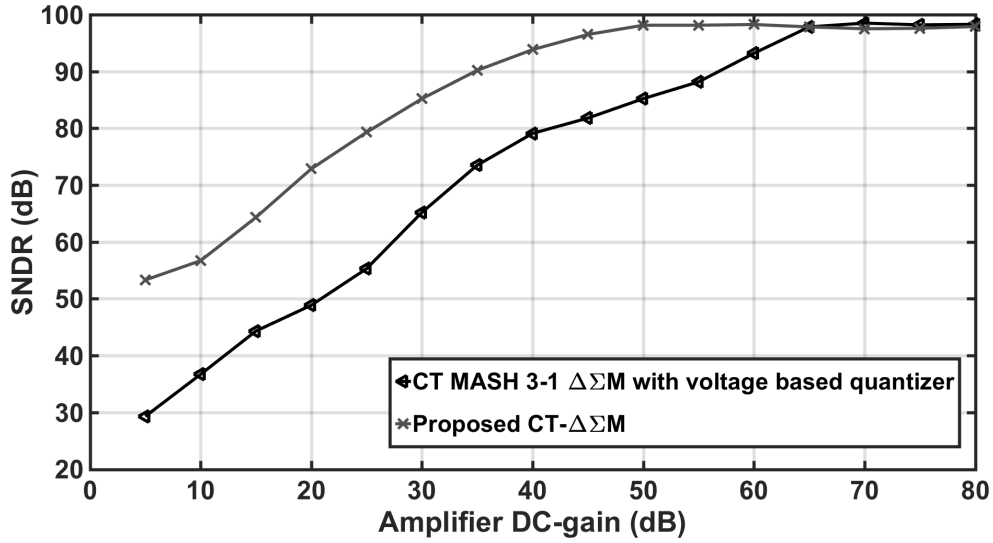
(a)



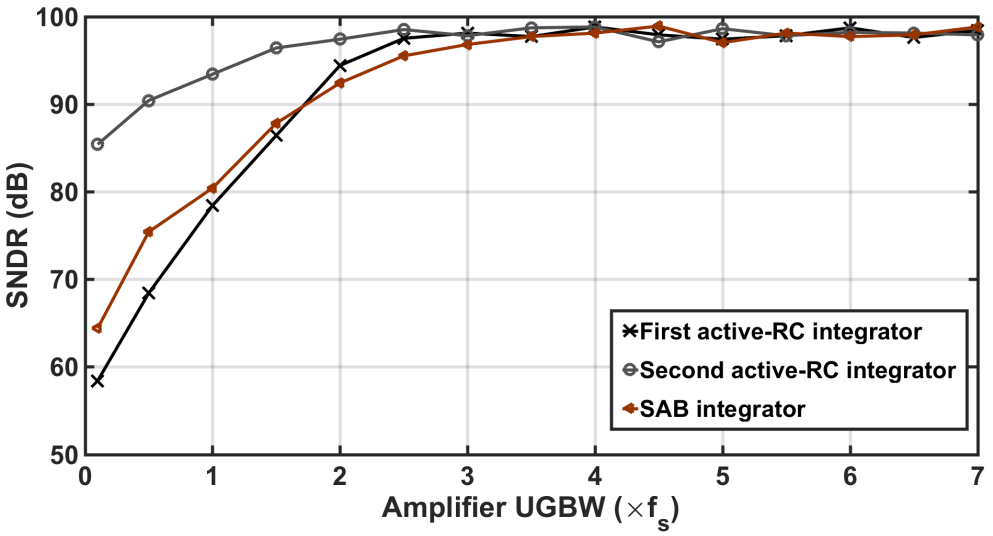
(b)

Figure 5.11 (a) SNDR as a function of supply voltage error in the PWM, (b) SNDR versus comparator delay.

delay is longer than the period of the carrier frequency, the comparator will make a wrong decision, while small delay, compared to the carrier period, has a negligible effect on the performance of the system. Fig. 5.11(b) shows the SNDR of the modulator as a function of the comparator delay extracted from electrical simulations. It is shown that the modulator is insensitive to the comparator delay up to 10% of the sampling period. Beyond this value, however, a performance degradation is observed. Nevertheless, this delay is added to the overall ELD, which can be compensated in practice by the action of the extra DAC used to this purpose.



(a)



(b)

Figure 5.12 Effect of loop-filter non-ideal effects : (a) Finite amplifier DC-gain, (b) amplifier UGBW.

5.5.6 Loop-filter non-idealities

The proposed modulator includes the second-order loop filter made up of active-RC integrators as will be described in next section. In addition to the thermal noise, which needs to be considered at transistor-level design in order to keep the in-band noise power according to the required resolution, other loop-filter non-idealities are the finite DC gain and the finite Unity Gain-BandWidth (UGBW). Fig. 5.12(a) illustrates the effect of finite amplifier DC gain on the proposed CT-ΔΣM extracted from electrical macro-model simulations in Cadence Spectre®. The DC-gain requirement of a conventional CT MASH ΔΣM with

voltage-based quantizer is shown as well for comparison purposes. As shown, the DC-gain requirement of the proposed modulator is about 50-dB, which is relaxed as compared to that required in a conventional modulator. That is justified by the fact that the GRO quantizer itself shows a relatively high SNDR and therefore a high-gain operational amplifier is not required in the proposed modulator.

The effect of UGBW is shown in Fig. 5.12(b). Note that the active-RC integrators used in this modulator require an amplifier with a UGBW of $2.5f_s$ and $1.5f_s$ for the first and the second integrators, respectively. To examine the effect of reducing the number of amplifiers in the proposed modulator, the loop-filter is also realized with a single amplifier biquad (SAB). Fig. 5.12(b) shows that an amplifier with a UGBW of about $3f_s$ is needed to implement the SAB integrator. Although the SAB integrator requires a slightly higher UGBW, it provides a better solution for high-speed CT-$\Delta\Sigma$M when it comes to power consumption and chip area [101].

5.6 Circuit Implementation

Figure 5.13 shows the schematic of the proposed GRO-based quantizer CT-$\Delta\Sigma$M. The front-end stage consists of a second-order loop-filter, realized by active-RC integrators, followed by a PWM and a GRO-TDC. The main DAC, i.e. DAC_1, is a Return-to-Zero (RZ) DAC and the auxiliary DAC, i.e. DAC_2, is realized with Non-Return-to-Zero (NRZ) DAC for ELD compensation. Note that the first stage is designed to accommodate one-clock cycle ELD while RZ waveform provides a half delay of extra room [30].

As mentioned earlier, active-RC integrators are used to meet the linearity requirements. Note that a small input resistor, R_{int1}, must be chosen to lower the thermal noise level as input-referred thermal noise of the active-RC integrator is proportional to the square of the integrating resistance. However, for a lower resistor value, a larger integrating capacitor is required resulting in stringent requirements on the amplifier. That being said, the first integrator resistor is opted to be 900-Ω resulting in an input-referred thermal-noise floor 91.2-dB below full scale range and corresponding integrating capacitor of 3-pF. The second integrator thermal noise however is suppressed by the gain of loop-filter. Therefore, the second integrator resistor, R_{int2}, is up-scaled to 14.4-kΩ to down-scale the second integrating capacitor to a value of 0.5-pF and hence relax the second amplifier requirements.

In the active-RC integrators, time constant and hence gain coefficients are defined by $R_{int}C_{int}$ products and deviations of integrator gain coefficient from its nominal values due to variation in technological process parameter influences the performance of the $\Delta\Sigma$M. To overcome

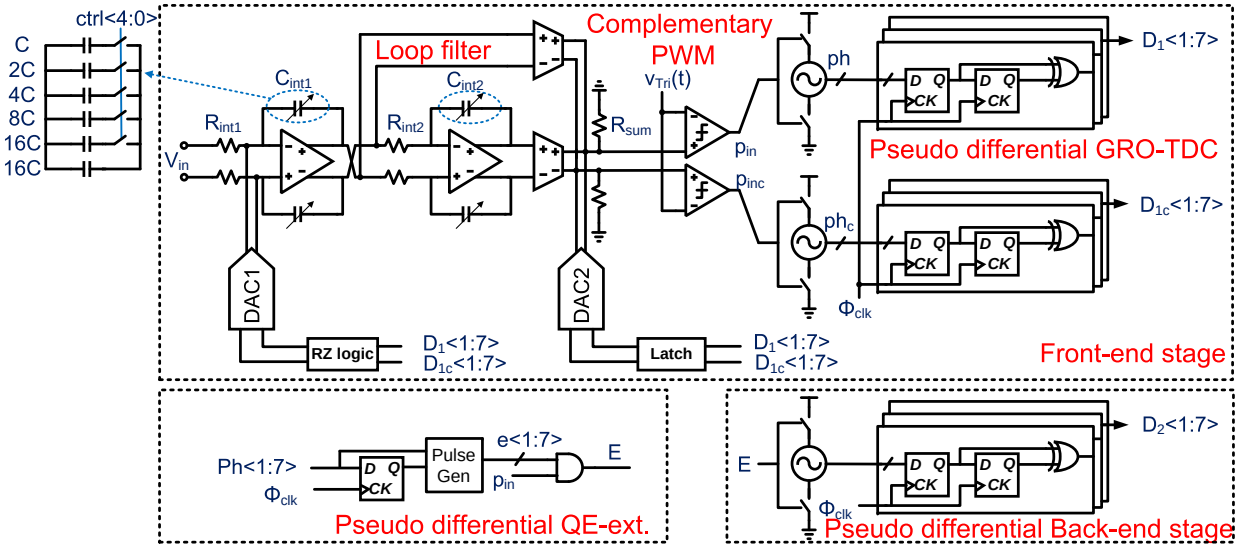


Figure 5.13 Circuit schematic of the proposed GRO-based CT MASH 3-1 $\Delta\Sigma$.

this issue, a 5-bit binary-weighted tunable capacitor array is employed for the integrating capacitors. For instance, capacitor array of the first integrator consists of a 1.5-pF "always-in-use" capacitor while the "total-in-use" capacitor is 4.4-pF. This results in a tuning range of 2.9 and a tuning resolution of 3.125%.

A pseudo differential PWM is adopted to translate the output voltage of the loop-filter into the time-domain information [21]. An external carrier signal is provided for the test-chip to have sufficient controls on the amplitude and frequency of the carrier signal. The carrier signal has a triangle waveform oscillating at f_s with an amplitude of 1-$V_{p\text{-}p}$. A 7-stage GRO-TDC is designed for both front-end and back-end stages. As described in Section 5.4, a digital circuit, i.e. QE-ext block, extracts the residue pulse from the front-end stage and feeds into the back-end GRO-TDC. An off-chip DCL is utilized to combine the outputs of two stages and cancel out the quantization error of the first stage. More details on the circuit implementations are provided in the following sections.

5.6.1 Operational Amplifiers

To minimize the ELD caused by the integrators, a high gain bandwidth product operational amplifier (op-amp) is utilized. To this end, a 3-stage amplifier with no-capacitor feedforward (NCFF) scheme is adopted [102] in this design, as shown in Fig. 5.14(a). Note that the NCFF op-amp is a power efficient architecture, compared to a Miller-compensated op-amp, since it avoids using extra power to charge and discharge the Miller capacitors. In other words, if

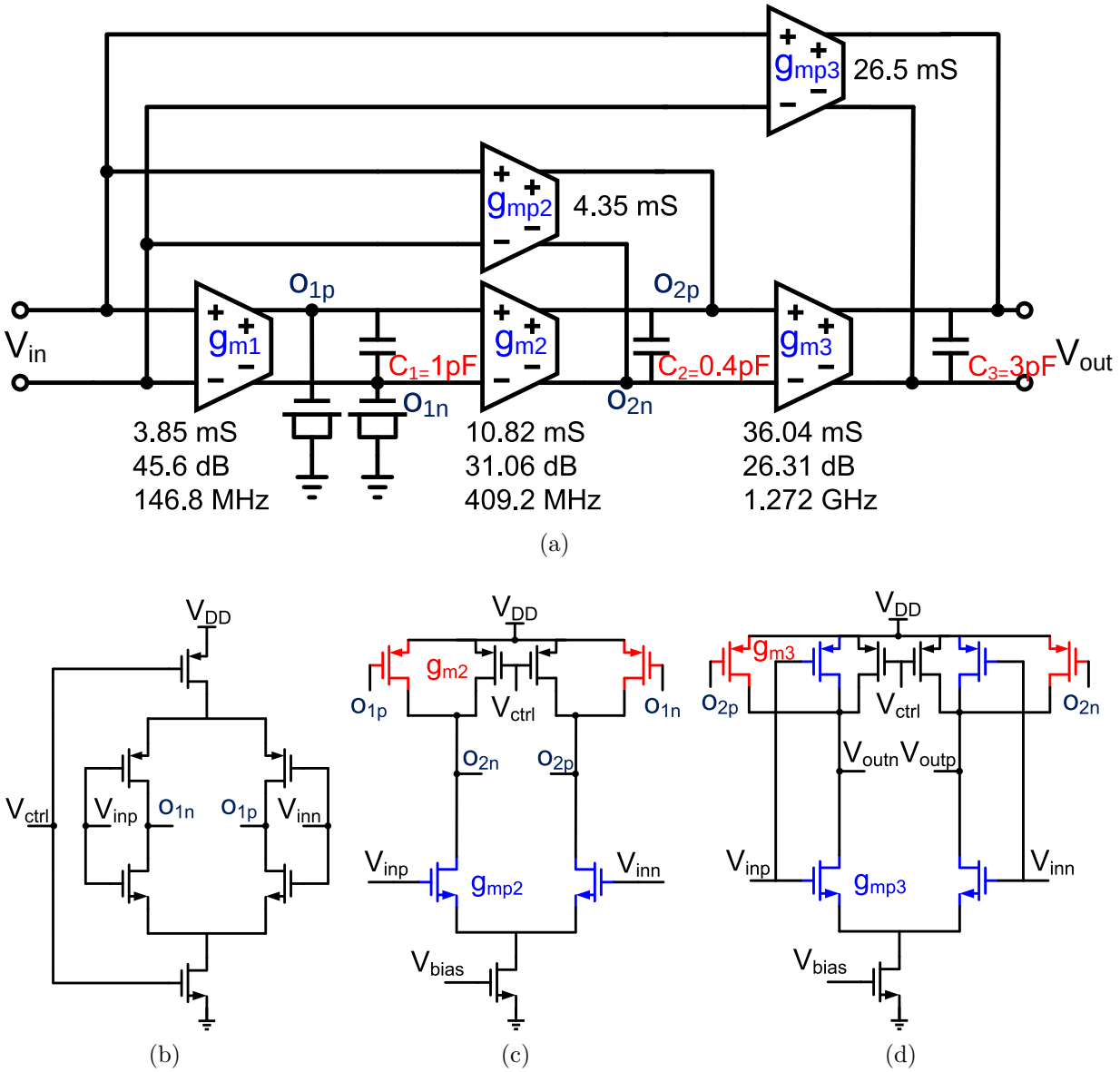


Figure 5.14 (a) Schematic of the operational amplifier including the design parameters, (b) Schematic of g_{m1}, (c) Schematic of $g_{m2,mp2}$, (d) Schematic of $g_{m3,mp3}$.

a Miller-compensated op-amp was used, the op-amp would need extra power to push non-dominant poles out of gain bandwidth. In the proposed op-amp, the high-gain path includes g_{m1}, g_{m2} and g_{m3} and they generate three poles. The high-speed path is provided by g_{mp2} and g_{mp3} where they introduce two Left-Half-Plane (LHP) zeros. These zeros cancel out two of the three poles and guarantee the stability of the op-amp.

Figure 5.14(b-d) shows the transconductance (gm) cells used in the op-amp. A self-biased inverter-based transconductor topology is utilized in the first stage of the op-amp. Since both NMOS and PMOS transistors contribute to the overall transconductance it helps to lower

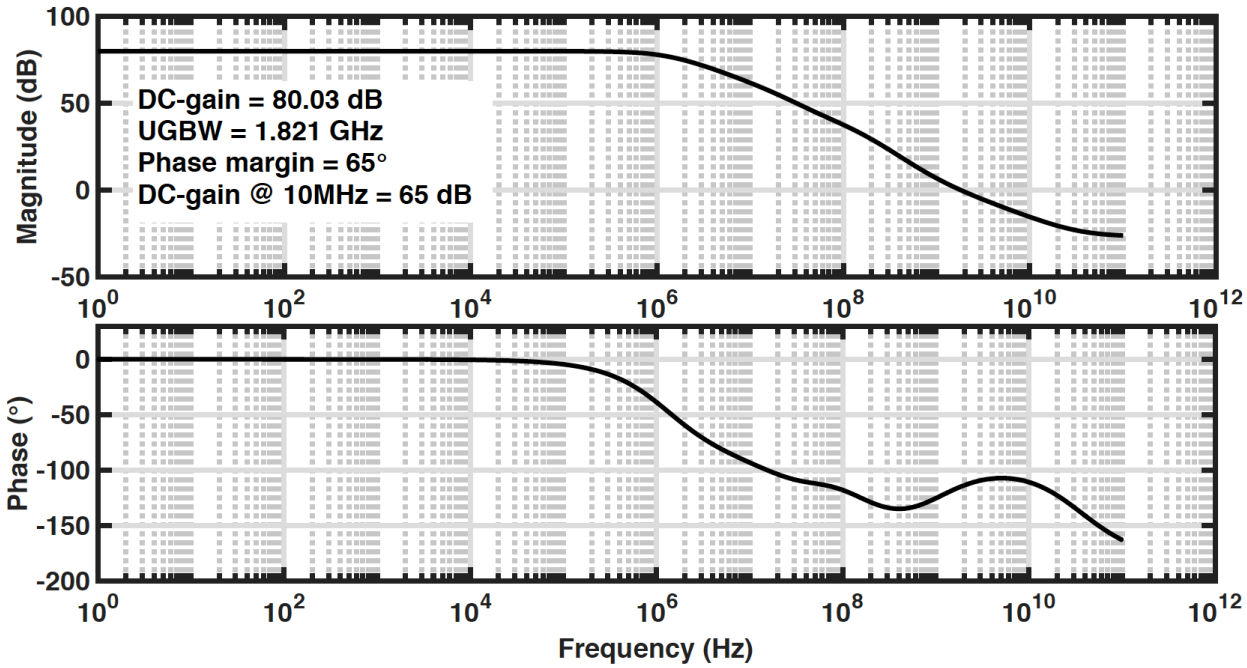


Figure 5.15 Frequency response of the first op-amp.

the intrinsic noise compared to that of single-stage, telescopic, folded-cascode, two-stage and current mirror transconductance amplifiers [54]. It also provides a DC-gain of 45.6-dB where suppresses the noise contribution of the following stages, i.e. $g_{m2,3}$. MOS capacitors are intentionally added at the output of g_{m1} to lower the bandwidth. The middle stage of the amplifier includes $g_{m2,mp2}$ where it provides a gain of about 31-dB. Not only does the last stage of the amplifier, i.e. $g_{m3,mp3}$, provide the high-speed path but it also takes the advantage of class-AB configuration to increase the driving capability. Note that $g_{m3,mp3}$ are the main contributors to widen the bandwidth of the op-amp. They, hence, provide transconductances of 36-mS and 26.5-mS, respectively. All stages also include common-mode feedback, not shown in the figure for simplicity, to set common-mode level to mid-supply, i.e. 0.5-V.

Figure 5.15 depicts the post-layout simulation of the first amplifier, featuring an 80-dB DC-gain, 65-dB gain at 10-MHz, a unity-gain-bandwidth (UGBW) of 1.82 GHz and a phase margin of 65°. Similar topology is employed for the second RC-integrator featuring a DC-gain of 76.12 dB, a UGBW of 1.03 GHz and a phase margin of 65.7°. Note that the power consumption of the second op-amp is almost $\frac{1}{3}$ of the first op-amp since its noise contribution is less. Therefore, it helps to diminish the overall power consumption.

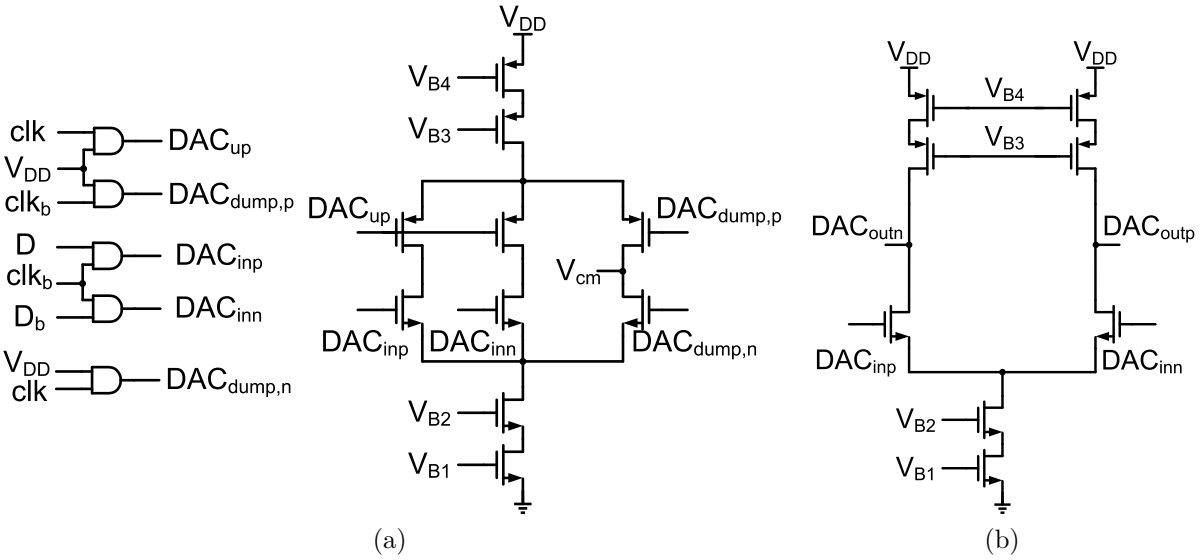


Figure 5.16 DAC cells, (a) DAC_1 and its RZ logic, (b) DAC_2.

5.6.2 Feedback DACs

As depicted in Fig. 5.13, the proposed ΔΣM incorporates two DACs, i.e. DAC_1 in the main path and DAC_2 for ELD compensation. As mentioned earlier and shown in Fig. 5.16(a), a RZ waveform is used for the main DAC to allow an additional compensation for ELD at the expense of sensitivity to the clock jitter. It includes an external voltage of $\frac{V_{DD}}{2}$ to keep the common mode level at mid-supply voltage. Large off-chip capacitors are used for both NMOS and PMOS bias voltages to diminish the noise coupling from the current reference. DAC_2 is realized with a NRZ pulse shape. The requirements for the second DAC is relaxed since the sensitivity to clock jitter and Inter-Symbol-Interference (ISI) is suppressed by the loop filter. To meet the linearity requirement and matching, lay-out strategies such as dummy transistors and common-centroid technique are used.

5.6.3 GRO-based Quantizer

Figure 5.17 illustrates the conceptual schematic of the GRO-TDC. Note that a pseudo-differential configuration is used although single-ended scheme is shown for simplicity. A 7-stage multi-path structure, representing a 3-bit quantizer, is used [82]. By doing so, the effect of leakage current and charge redistributions can be reduced resulting in a reduction of gating clock skew. The GROs are laid-out in an inter-woven structure to obtain a higher level of matching. By doing so, their mismatches are averaged out. Always-on buffers are used at the output of GRO phases to isolate GRO from the FDC kick-back noise. It also

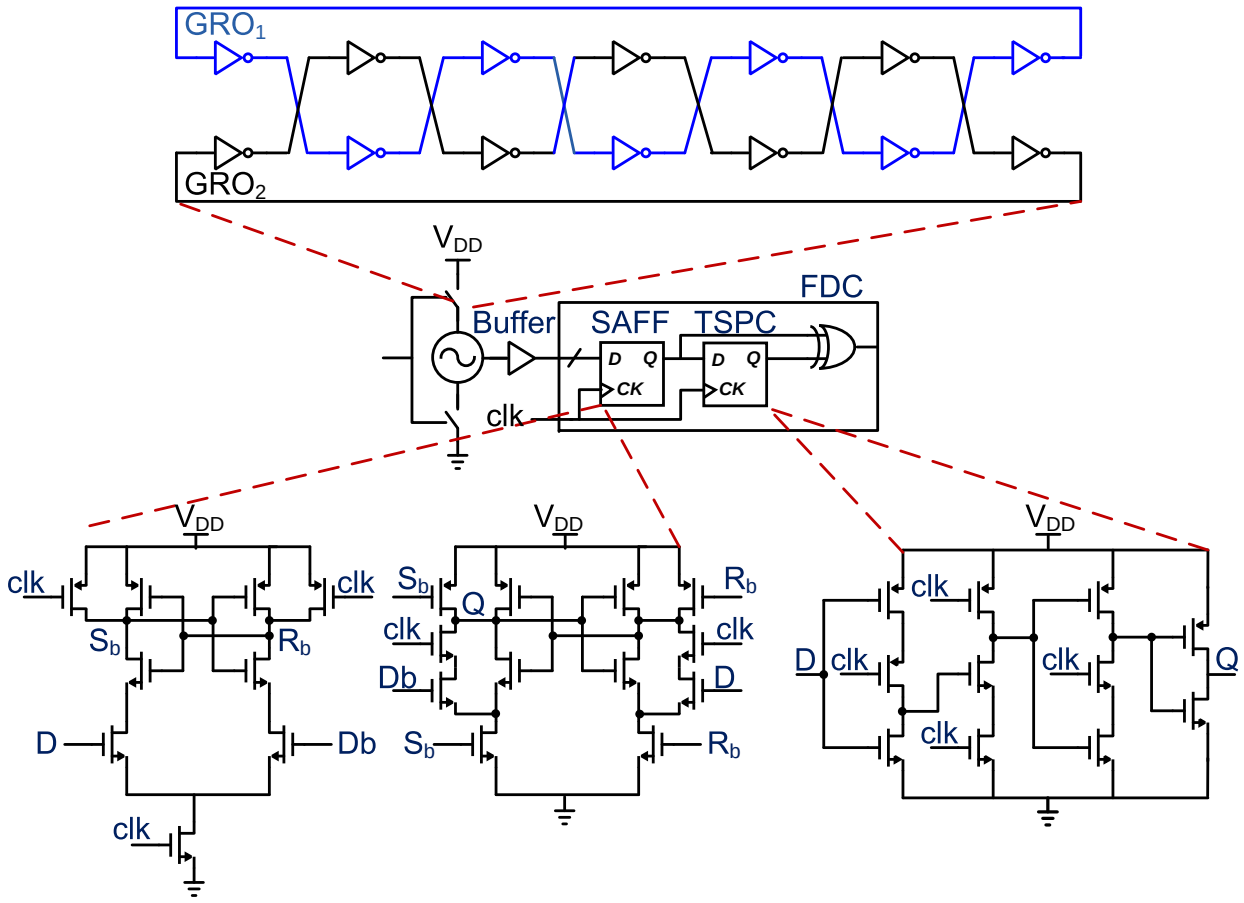
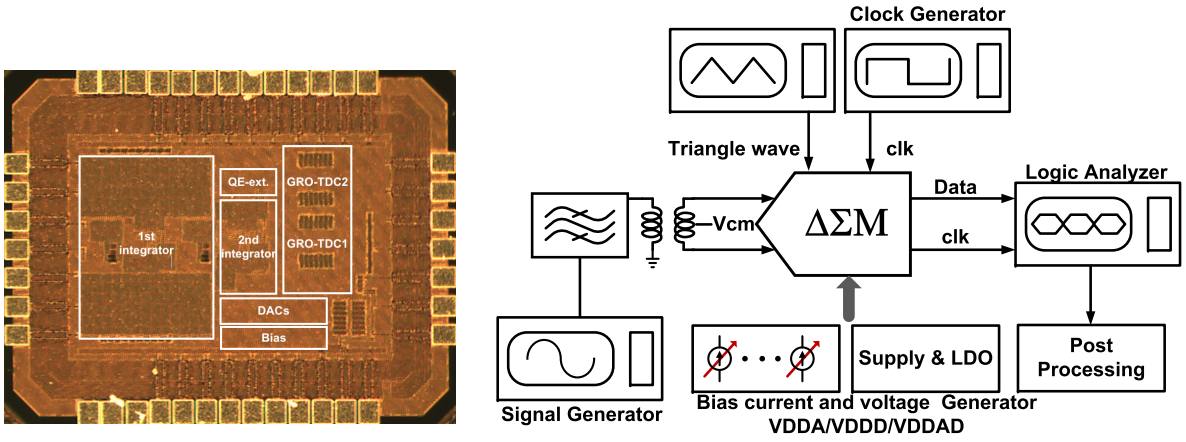


Figure 5.17 Schematic of GRO-TDC, (top) An inter-woven GRO structure, (middle) GRO-TDC including GRO and FDC, (bottom) Circuit level schematic of SAFF and TSPC.

sharpens the rising and falling edges of the GRO output to alleviate rising/falling edges' distortion dependent. Variable capacitors are used to control the oscillation frequency of the GRO. Post-layout simulation of the GRO shows a phase noise of -80 dBc/Hz at 1-MHz offset frequency. Shown in the bottom side of Fig. 5.17, sense amplifier flip-flop (SAFF) and true sample phase clock register (TSPC) are employed for the first and the second flip-flop in the FDC, respectively [50]. The SAFF shows a metastability of less than 1-ps which makes it appropriate for high resolution GROQ. However, the metastability is not a concern for the second flip-flop in the FDC. Therefore, the TSPC is used to further diminish the power consumption. Finally, standard cells are employed to realize the digital gates.



(a) (b)

Figure 5.18 (a) Chip micrograph, (b) Measurement setup.

5.7 Measurement Results

The proposed GRO-based quantizer CT MASH ΔΣM has been fabricated in a 1P8M 65-nm CMOS technology. Three different supply voltages are used to supply analog, digital and mixed-mode blocks. To protect the analog blocks from the noise inducted by digital circuits, guard rings are used. The op-amps are implemented with standard CMOS devices and RF devices are used to implement the GROs. The layouts of the building blocks are designed fully symmetrical, when applicable, to match their differential signal paths.

Figure 5.18(a) shows the chip micrograph. A 44-pin QFN package is used to package the die. As depicted, almost 50% of the chip is occupied by the first integrator while two GROQs only spend less than 20% of the total area. Fig. 5.18(b) shows the measurement setup. A single-ended input sinewave is band-pass filtered with a passive band-pass circuit to suppress the harmonics of the signal generator and then converted to a differential signal using a balun. The clock signal is generated by a pattern generator and the digital outputs are stored in the memory of an oscilloscope and then transferred to a PC for subsequent processing in MATLAB.

Figure 5.19 shows the spectrum of the proposed modulator with a half-scale (−6-dBFS) input tone located at 2.4-MHz while clocked at a sampling frequency of 640 MHz. The SNR and SNDR of the modulator versus input signal level are shown in Fig. 5.20. The modulator achieves an 81.5-dB peak SNR at −2.2-dBFS, 79.2-dB peak SNDR at −4-dBFS and an 80-dB DR from a 1-V supply. Therefore, the corresponding Schreier and Walden FOMs, as defined

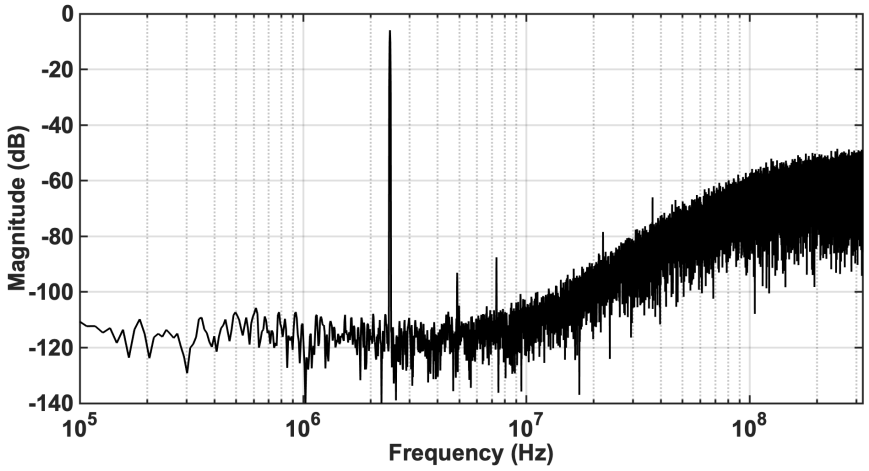


Figure 5.19 Measured PSD of the proposed CT MASH ΔΣM.

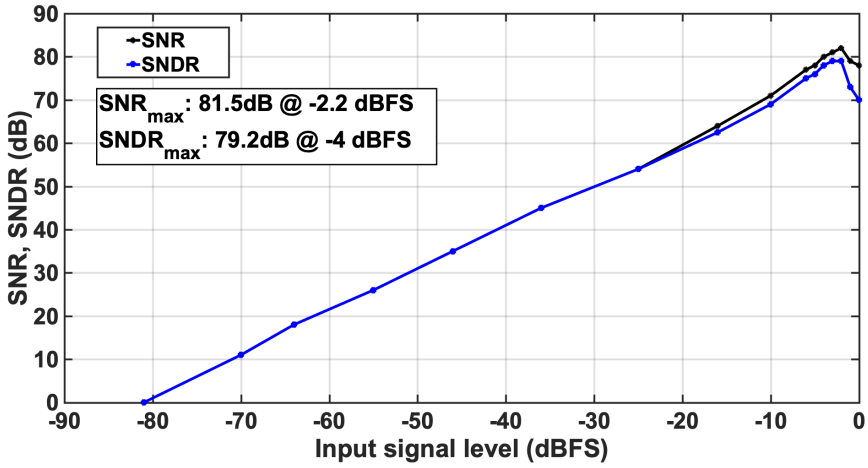


Figure 5.20 Measured SNR and SNDR versus input signal level.

in (5.6) and (5.7), are 169-dB and 80.5-fJ/step, respectively.

$$FOMS = DR + 10\log(\frac{BW}{Power}) \tag{5.6}$$

$$FOMW = \frac{Power}{2 \cdot BW \cdot 2^{\frac{SNDR-1.76}{6.02}}} \tag{5.7}$$

Figure 5.21 depicts the power breakdown of the proposed ΔΣM. As shown, The first op-amp dissipates about 45% of the total power while the second op-amp contributes about 16% of the total power. Two GROQs totally consumes 1.3-mW which is about 11% of total power budget. The main DAC, i.e. DAC_1 consumes 1.6-mW where it is 13% of total power.

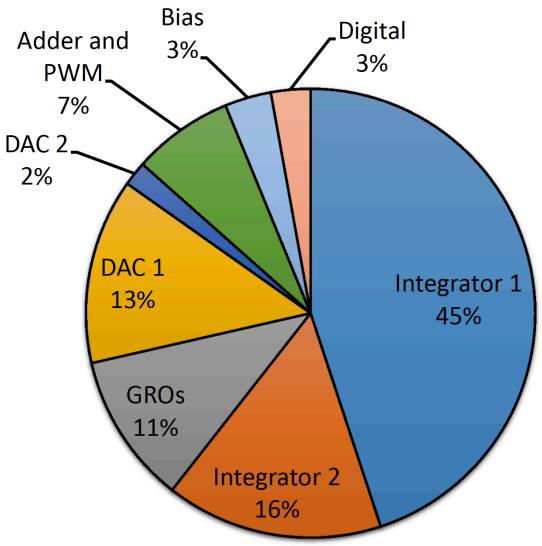


Figure 5.21 Power breakdown.

Table 5.1 Performance Summary and Comparison with the State of the Art all from Measurements

Ref. Architecture	[30] VCOQ	[31] VCOQ	[13] RC-VCOQ	[41] PWM-VCOQ	[87] VCOQ-CT	This work
Technology (nm)	130	130	90	90	65	65
BW (MHz)	10	20	10	8	10	10
Fs (MHz)	900	900	600	640	1600	640
SNR (dB)	86	81.2	79.1	61.1	66.2	81.5
SNDR (dB)	72	78.1	78	59.1	62.5	79.2
DR (dB)	72.1	80	83.5	65.6	71	80.3
Power (mW)	40	87	16	4.3	3.7	12
Area (mm^2)	1.69	0.45	0.36	0.1	0.01	1
FOMW (fJ/Conv.-step)	587	331	125	366	169.7	80.5
FOMS (dB)	159	164	166.3	158.3	165.3	169.2

Table 5.1 shows the performance summary of the proposed $\Delta\Sigma$M and compares it with the state of the art on VCO-based $\Delta\Sigma$Ms within the same range of signal-bandwidth application. The table does not include $\Delta\Sigma$Ms applied for TDCs such as those reported in [50] and [28]. To the best of the authors' knowledge, time-domain signal was used to characterize these data converters, which make the comparison with the works shown in Table 5.1 difficult and not fair. However, from the architectural-level point of view, the proposed architecture shows the following benefits compared to [50] and [28]. First, the voltage to time translator in the proposed architecture is placed inside the loop-filter and hence its non-idealities gets shaped by the loop-filter. Second, [50] and [28] are severely susceptible to the phase-noise of the GROs

while the proposed architecture is quite robust. Finally, note that the proposed modulator shows the best FOMW and one of the best FOMS among recently published VCO-based $\Delta\Sigma$Ms.

5.8 Conclusion

A new approach to implement CT MASH $\Delta\Sigma$Ms based on the use of GRO quantizers has been presented. The proposed topology allows to achieve a fourth-order noise-shaping by using a reduced analog circuitry content with only a second-order active-RC filter, implemented by the inverter-based multi-stage amplifiers. One of the key contributions is that the quantization error is extracted in time-domain, which allows to combine GRO-based quantization with conventional CT loop-filters while increasing the noise shaping by simply extending the number of stages in the case with GRO-based TDCs in a mostly-digital scaling-friendly approach. In order to probe the presented circuits and systems techniques, a cascade 3-1 $\Delta\Sigma$M has been designed and integrated in a 65-nm CMOS technology. Experimental results demonstrate the efficiency of the proposed $\Delta\Sigma$ converter, featuring a competitive performance with the state of the art. The presented strategies open the doors to implement high-order frequency-based CT-$\Delta\Sigma$Ms with higher linearity than previous approaches, benefiting from technology downscaling in terms of reduced propagation delay and potentially higher speed towards the GHz range.

CHAPTER 6 GENERAL DISCUSSION

The foundation of this thesis is based on the fact that not only are circuit-level techniques important to realize ΔΣMs, but it is also an indispensable fact that architectural solutions remarkably improve the performance of ΔΣMs. To demonstrates the importance of the above statement, three architectures are proposed while two of them have been silicon verified. The first two architectures, i.e. adder-less MASH ΔΣM and SMASH ΔΣM, are implemented in the voltage domain and the third one is realized in a hybrid voltage and time domain. It is also worth mentioning that the adder-less MASH ΔΣM and the hybrid ΔΣM are silicon verified in a 180-nm and 65-nm CMOS technology, respectively. The first one has been designed to cover 20-kHz signal bandwidth while the latter has been characterized to support 10-MHz signal bandwidth. A relatively old and inexpensive CMOS process i.e., 180-nm, is chosen to demonstrate the possibility of performing low-power design with old processes. The supply voltage is shrunken to a half of nominal voltage for the first design. A relatively advanced node CMOS process is hired to implement the hybrid ADC while the nominal supply voltage is utilized. A general discussion and observations associated with the proposed architectures are drawn as follows.

As mentioned in Chapter 3, ΔΣM based on the feed-forward path topology is preferred due to its low-distortion property. However, the summation block to sum up the feed-forward paths is the main bottleneck of this configuration. It must be noted that a high-speed OTA is required to implement the summation block which makes this architecture undesirable. Therefore, the idea is to eliminate this block without compromising the performance. In the first part of this thesis, an adder-less MASH ΔΣM is proposed. In the proposed topology the summation block is moved back to the input of the second integrator and hence the second integrator serves as an integrator and an adder simultaneously. Another feature of the proposed architecture is that quantization noise is extracted from the analog nodes of the modulator and there is no need to realize a DAC to do so any longer. In the circuit level phase, a self-biased inverter-based OTA is first proposed while biasing it in the weak-inversion region. Weak-inversion region offers an interesting region to perform low-power design due to a higher $\frac{g_m}{I_D}$. It is observed that the DC-gain of the proposed self-biased OTA is robust over PVT variations while the unity gain bandwidth and slew rate fail over slow-slow corners and low supply voltage. To fix this issue a self body biased inverter-based OTA is then proposed. Analysis shows that the performance metrics of the proposed OTA is robust over PVT variations. The circuit is fabricated in 0.18-μm CMOS technology. The prototype achieves a SNR, SNDR and DR of 88.7 dB, 86.4 dB and 91 dB, respectively. The circuit consumes

103.4-μW at a 0.9-V supply voltage, exhibiting a cutting-edge performance in comparison to the state of the art.

It is mentioned in Chapter 3 that the proposed adder-less MASH $\Delta\Sigma$M shows a better power efficiency compared to [67] and [71]. Modulators proposed in [67] and [71] consume 2.2 and 3 times power while offering only 3.5-dB and 4.8-dB better FOM_{DR} than this work. Note that the first one is a single-bit MASH 2–1 and the latter is a single-bit single-loop third order $\Delta\Sigma$M. Taking the advantages of the weak-inversion region, the proposed $\Delta\Sigma$M shows a 12-dB improvement in PSRR compared to that proposed in [67] although the worst case PSRR is the positive PSRR for a 2% mismatch of NMOS transistors. Gain-boosted technique is utilized in [67] at the expense of added power consumption and circuit complexity. However, it is shown that the proposed topology needs only 50-dB OTA DC-gain and it is met by the proposed SBB inverter-based OTA. Therefore, neither gain-boosting technique nor complex PVT compensation techniques are required. Unlike [55], the proposed OTA is biased in a weak-inversion region resulting in lower thermal noise and power consumption. Moreover, the proposed SBB inverter-based OTA meets the specifications at the SS process corner as well as low supply voltage. Although the $\Delta\Sigma$M proposed in [16] shows a better power efficiency, it is essentially due to the lower supply voltage leading to somewhat reduced DR.

Among the main features of the proposed adder-less MASH $\Delta\Sigma$M, the downside of the proposed architecture is the SNDR degradation caused by mismatch between the analog loop-filter and the digital cancellation logic. As a matter of fact, not only does the proposed topology suffer from this downside but also every MASH structure. It is observed that a calibration on the digital cancellation logic is needed to retrieve the performance of the modulator. To overcome this issue, a modified adder-less SMASH $\Delta\Sigma$M is proposed, as described in Chapter 4. The STF of the proposed SMASH $\Delta\Sigma$M is restored to unity which makes the proposed architecture robust to OTA nonlinearity while showing a quite relaxed OTA DC-gain. Unlike the conventional SMASH structure, quantization error of the first stage is fully canceled in the proposed architecture. As a consequence, the interstage gain can now increase the performance of the proposed modulator. All above-mentioned characteristics make the proposed architecture suitable for low-voltage, low-power and high-speed applications. This architecture has not been silicon verified because of limited design time. Finally, modifying the proposed topology in Chapter 3 to that presented in [61], could help to lower the OTA DC-gain. In that case, the modulator in [61] is re-analyzed for an OSR of 128 and it is observed that a 20-dB OTA DC-gain is sufficient to keep IBN_{max} intact, outlining a potential improvement strategy to attain a lower critical OTA gain value.

Either shrinking the supply voltage or using advanced node CMOS processes make the design

of the analog circuits cumbersome specially when high-speed applications are targeted. This is due to the limited voltage headroom to bias the circuits e.g. op-amps in the strong-inversion region. Time domain signal processing offers appealing features to realize analog and mixed signal functions without being concerned about the voltage headroom. Pure time domain signal processing, however, has it own disadvantages. The main one is that most signals are in voltage and current domains and to perform time domain signal processing they need to be translated into the time domain. Such translation, unfortunately, is a very non-linear conversion and severely degrades the performance of the analog building blocks. The concept of feedback can save time domain signal processing from being deprived of using to realize the analog blocks. Fortunately, $\Delta\Sigma$Ms are also founded based in the feedback concept. Having discussed from that point of views, the motivation of the third proposed architecture is to use time domain analog blocks inside a feedback system (for example $\Delta\Sigma$M in this research) to alleviate its non-linear behavior.

VCO-based quantizer is a time-domain system where the voltage/current signal is converted to the frequency/time domain by a VCO. The output phases of the VCO are then quantized. The main downside of the VCO-based quantizer is a severe non-linearity of the VCO voltage-to-frequency transfer characteristic. GRO-based quantizer can help to alleviate such non-linearity. However, there is still a non-linear block, i.e. PWM, in this topology. The implementation of CT MASH $\Delta\Sigma$Ms with multi-bit GROQs in all stages is considered in this research to overcome the drawbacks of the VCO-based quantizer. A PWM followed by a GRO-based TDC is used as a quantizer inside the loop-filter of a CT $\Delta\Sigma$M. Therefore, the non-linearity issue of the PWM is alleviated. Moreover, this strategy allows to extract the quantization error in a more robust way in order to build cascade topologies where the back-end stages are simple GRO-based TDCs, thus allowing to build high-order mostly-digital $\Delta\Sigma$Ms. The quantization error of the first stage is already available in the time domain. Therefore, it is extracted and fed into the back-end GRO-based TDC in a mostly-digital scaling-friendly way. Note that quantization error extraction is troublesome in the voltage-mode CT MASH $\Delta\Sigma$Ms [95] since they need a relatively complex circuit to estimate the quantization error.

The proposed circuit has been fabricated in a 65-nm CMOS technology with 1-V supply voltage. The chip prototype operates at 640-MHz sampling frequency to digitize 10-MHz signals. To the best of the author's knowledge, this is the first reported experimental demonstration of a GRO-based CT MASH $\Delta\Sigma$M, featuring an 81.5-dB SNR at -2.2-dBFS, a 79.2-dB SNDR at -4-dBFS and a dynamic range (DR) of 80 dB, with a power consumption of 12-mW. These metrics demonstrate state-of-the-art performance, with a Walden FOM of 80.5 fJ/conv-step and a Schreier FOM of 169.2 dB, thus demonstrating the benefits of the

proposed GRO-based $\Delta\Sigma$ modulation technique.

As tabulated in Chapter 5, table 5.1 summarizes the performance of the proposed $\Delta\Sigma$M and compares it with the state of the art on VCO-based $\Delta\Sigma$Ms within the same range of signal-bandwidth application. The proposed architecture demonstrates efficient FoMs compared to the first generation of the VCOQ $\Delta\Sigma$Ms [30, 31]. When it comes to comparing with [13], both architectures are showing almost a similar performance in terms of dynamic measurements. However, the proposed modulator dissipates less power than [13]. It is essentially due to the fact that a power hungry FLASH ADC is used in an RC-VCOQ structure. Although an efficient foot-print and low-power design has been addressed in [87], it still suffers from a limited dynamic performance. Table 5.1 does not include $\Delta\Sigma$Ms applied for TDCs such as those reported in [50] and [28]. Since time-domain signal was used to characterize these data converters, which make the comparison with the works shown in Table 5.1 difficult and not fair. However, from the architectural-level point of view, the proposed architecture shows the following benefits compared to [50] and [28]. First, the voltage to time translator in the proposed architecture is placed inside the loop-filter and hence its non-idealities gets shaped by the loop-filter. Second, [50] and [28] are severely susceptible to the phase-noise of the GROs while the proposed architecture is quite robust. Finally, It is worth noting that the DT version of the proposed modulator is first proposed in [94] by the author. However it is limited in practice by the transient response of the DT loop filter used in the front-end stage, the modulator presented in this research embeds a GRO-based TDC in a CT MASH $\Delta\Sigma$M, thus benefiting from the combination of power-efficient CT loop filter and the inherent linearity of GRO-based quantization.

CHAPTER 7 CONCLUSION AND RECOMMENDATIONS

7.1 Conclusion

ADCs are known as once of the main building blocks in signal conditioning to translate analog signals into the digital domain to perform post processing. Having a small footprint and low power ADC is one of the main challenges in the advanced node processes. Among variety of ADC, $\Delta\Sigma$Ms are the most appropriate solution for low/medium frequency and high resolution applications. $\Delta\Sigma$Ms also help to realize a data converter with low precision analog blocks due to the noise shaping property. Special cares, however, must be taken into account when realizing a $\Delta\Sigma$M in the advanced node processes. To overcome the drawbacks of realizing such ADCs, seeking architectural solutions is crucial. To do so, proper approaches can be found to improve the efficiency of a $\Delta\Sigma$M at the system level. Once found, circuit level techniques help to further improve the efficiency of the $\Delta\Sigma$Ms. The main objectives of this research are first seeking architectural solutions to realize $\Delta\Sigma$Ms and the second is proposing appropriate circuit level techniques.

Having discussed from that point of view, different architectures are proposed in a pure voltage domain as well as a hybrid voltage and time domain signal processing. To do so, an adder-less MASH $\Delta\Sigma$M is proposed where the power hungry summation block is eliminated and the second integrator in the proposed topology serves simultaneously as an integrator and an adder. Quantization error can be extracted through the analog signals without employing any additional DAC. The proposed modulator is silicon verified with 0.18-μm CMOS technology. To realize the OTA used in the proposed modulator a self and body biased inverter-based OTA, operating in the weak-inversion, is proposed while presenting lower thermal nosie compared to other topologies. The prototype achieves a SNR, SNDR and DR of 88.7 dB, 86.4 dB and 91 dB, respectively. The circuit consumes 103.4-μW at a 0.9-V supply voltage, exhibiting a cutting-edge performance in comparison to the state of the art.

It is found that although MASH $\Delta\Sigma$M can offer a high resolution ADC it suffers from a mismatch between analog loop-filter and digital cancellation logic. Such mismatch degrades the performance of a MASH $\Delta\Sigma$M if it is not properly considered. To overcome such a drawback an adderless SMASH $\Delta\Sigma$M based on a feed-forward loop filter is proposed. In the proposed architecture, the digital cancellation logic is eliminated and so does the source of the problem.

Although, the previous proposed architectures are mainly based on a voltage mode signal

processing, the time domain signal processing is another venue to realize analog building blocks such as ADCs, filters, etc. It is observed that a hybrid domain (voltage and time) helps to take the advantages of both domain without being restricted by headroom in the voltage domain or non-linearity in the time domain. To do so, a GRO-based MASH structure $\Delta\Sigma$M is proposed in which part of the design is shifted to the highly scalable digital domain. The proposed modulator consists of a front-end stage where a second order loop-filter followed by a GRO-TDC realizes a third order $\Delta\Sigma$M. The quantization error is simply extracted in the digital domain by a digital circuit. The error then feeds the back-end stage to form a MASH 3-1 $\Delta\Sigma$M. Therefore a scaling-friendly architecture is proposed. The proposed architecture is implemented in 65-nm CMOS technology while the supply voltage is 1-V.

7.2 Research contributions

The main contribution of this research is seeking architectural as well as circuit level solutions to tackle the limitations of $\Delta\Sigma$Ms in advanced node CMOS technologies. To do so, different architectures are proposed and two of them are silicon verified in 0.18-μm and 65-nm CMOS process. The contributions are detailed as follows :

1. Implementation of an adder-less MASH $\Delta\Sigma$M for a 20-kHz signal bandwidth with a supply voltage of 0.9-V in an 0.18-μm CMOS technology. Conventional feed-forward topology is modified to eliminated the power-hungry adder. A direct feed-forward path is also added to the proposed topology to have an STF of unity. Therefore, at the architectural level, an OTA and two OTAs are saved for the second order an MASH 2-2 $\Delta\Sigma$Ms, respectively.
2. In the proposed architecture, the quantization error is extracted by proper combination of the input signal, output of the first integrator, and output of the third integrator. Unlike the conventional approach, the proposed solution make the realization of a MASH $\Delta\Sigma$Ms easier such that it is well-appropriate for multi-bit quantizer.
3. A self-biased inverted-based OTA biased in the weak inversion is proposed. It is known that circuits, biased in the weak inversion, fails at slow process corners or low supply voltage. To overcome that issue, a self and body-biased OTA is proposed. It is demonstrated that the proposed OTA offers a stable DC-gain while meeting the requirements over PVTs.
4. MASH architectures are always suffering from mismatch between analog loop-filter and digital cancellation logic and hence degrading the performance of the MASH $\Delta\Sigma$M. To address this issue, a modified SMASH $\Delta\Sigma$M is proposed at the architectural level.

It is shown that the proposed topology is no longer sensitive to the mismatch and gain requirements to implement the OTAs are quite relaxed. The proposed topology also shows a better linearity compared to those of conventional SMASH and feed-forward SMASH.

5. One of the main concerns in the voltage domain is being limited by voltage headroom. To address that issue, a scaling-friendly architecture based on a hybrid voltage and time domain is proposed. It is worthwhile to count the advantages of the proposed architecture. (1) Part of the design is shifted to the time domain while a fourth order noise-shaping where a second order noise-shaping is provided through the voltage domain signal processing and another second order noise-shaping is given by the time domain signal processing. (2) The GRO-TDC in the proposed topology is inherently linear while the PWM is implemented in a highly-linear way. (3) The proposed modulator does not need an explicit dynamic element matching techniques for the front-end stage hence it eases excess loop delay compensation. (4) Unlike the conventional CT-MASH $\Delta\Sigma$Ms, the quantization error represented in the time domain and it is extracted by a simple digital circuit. The combination of the above mentioned techniques makes the proposed architecture appropriate for advanced node CMOS processes. The Proposed GRO-based MASH $\Delta\Sigma$M is silicon-verified in 65-nm CMOS technology.

7.3 Recommendations for future work

Different architectures are presented in this thesis to overcome the limitations of the previous topologies. However, the gate is still open to scrutinize novel architectures. Also, new methods can be proposed to realize a $\Delta\Sigma$M in an efficient way at the circuit level. Some approaches are discussed as future work.

1. The modulator presented in Chapter 3, is implemented in the DT domain. However, it is recommended to follow similar approach to implement the modulator in the CT domain. Therefore, it will be a good option for higher bandwidth application e.g. GS/s $\Delta\Sigma$Ms.
2. The modulator proposed in Chapter 4, has not been silicon verified. The proposed architecture can be realized in advanced node CMOS technologies while using multi-bit quantizer. Therefore, the effectiveness of the proposed solution can be further discussed.
3. A CT GRO-based MASH $\Delta\Sigma$M is addressed in Chapter 5. As mentioned in Chapter 3, MASH structure $\Delta\Sigma$Ms are susceptible to mismatch between analog loop-filter and

digital cancellation logic. It is a good practice to implement the proposed CT GRO-based MASH ΔΣM through the SMASH architecture results in a better efficiency.

4. The op-amp utilized in Chapter 5 is based on multi stage no miller capacitor OTAs and conventional OTAs are used to realize the multi stage op-amp. However, inverter based OTAs result in a better power efficiency.
5. The loop-filter, realized in Chapter 5, is based on the active-RC integrators. However, using Single-Amplifier Biquadratic filter rather than active-RC integrator can substantially diminish power consumption.

7.4 Publication

7.4.1 Journal publications

— M. Honarparvar, J. M. de la Rosa, and M. Sawan, “A 10-MHz BW 79.2-dB SNDR 640-MS/s Continuous-Time Fourth-Order MASH ΔΣ Modulator Using GRO-based Quantization”, Submitted to IEEE Transactions on Circuits and Systems I : Regular Papers, Dec. 2018

— M. Honarparvar, J. M. de la Rosa and M. Sawan, "A 0.9-V 100-μW Feedforward Adder-Less Inverter-based MASH ΔΣ Modulator with 91-dB Dynamic Range and 20-kHz Bandwidth," in IEEE Transactions on Circuits and Systems I : Regular Papers, vol. 65, no. 11, pp. 3675-3687, Nov. 2018. doi : 10.1109/TCSI.2018.2854220

— M. Honarparvar, J. M. de la Rosa, F. Nabki and M. Sawan, "SMASH ΔΣM modulator with adderless feed-forward loop filter," in Electronics Letters, vol. 53, no. 8, pp. 532-534, 13 4 2017. doi : 10.1049/el.2016.4733

7.4.2 Conference papers

— M. Honarparvar, J. M. de la Rosa, F. Nabki and M. Sawan, "Design Considerations of MASH ΔΣ Modulators with GRO-based Quantization," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, 2018, pp. 1-5. doi : 10.1109/ISCAS.2018.8351290

— M. Honarparvar, J. M. de la Rosa, F. Nabki and M. Sawan, "Novel Band-Pass ΔΣ Modulators Based on a Modified Adder-Less Feed-Forward Structure," 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, 2017, pp. 1288-1291. doi : 10.1109/MWSCAS.2017.8053166

— M. Honarparvar, M. Safi-Harb and M. Sawan, "An amplifier-shared inverter-based MASH structure ΔΣ modulator for smart sensor interfaces," 2016 IEEE International

Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 2250-2253. doi : 10.1109/ISCAS.2016.7539031

— M. Honarparvar, R. Landry, F. Nabki and M. Sawan, "Advanced modeling technique for bandpass continuous-time delta-sigma modulators," 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS), Trois-Rivieres, QC, 2014, pp. 341-344. doi : 10.1109/NEWCAS.2014.6934052

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